

VEST i.MX8M Plus SOM Board Hardware Reference Manual

VEST-i.MX8M-PLUS-SOM-USG-001, REV C



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LIST OF ABBREVIATIONS

Acronyms	Abbreviations
APC	Advanced Products Corporation Private Limited
ARM	Advanced RISC Machine
CAN	Controller Area Network
CSI	Camera Serial Interface
DSI	Display Serial Interface
eCSPI	Enhanced Configurable Serial Peripheral Interface
eMMC	embedded Multi-Media Card (MMC)
GB	Giga Byte
GPIO	General Purpose Input Output
HDMI	High-Definition Multi-media Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
ISO	International Organization for Standardization
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signal
MB	Mega Byte
Mbps	Megabits per second
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
NC	Not Connected
PWM	Pulse Width Modulation
PCIe	Peripheral Component Interconnect Express
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SJC	System JTAG Controller
SOM	System On Module
SOC	System-on-a-Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	Universal Serial Bus on the Go
V*EST	Venture Embedded Solutions Technology "The Logo"
VEST	Venture Embedded Solutions Technology

Table 1-1: List of Abbreviations

REFERENCE DOCUMENTS

- [*i.MX8M Plus Application Processor Datasheet*](#)
- [*i.MX8M Plus Application Processor Reference Manual*](#)
- [*i.MX8M Plus Hardware Developer's Guide*](#)
- [*i.MX8M Plus Product Lifetime Usage*](#)

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1 OVERVIEW

1.1 GENERAL INFORMATION

The VEST i.MX8M Plus SOM (System-On-Module) is based on the NXP's i.MX8M Plus ARM® Cortex™-A53 processor. The SOM provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics, and video capabilities, as well as high-processing, compact, cost effective and with low power operation.

The VEST i.MX8M Plus SOM board runs on the following Operating System:

- Embedded Linux
- Yocto

1.2 FEATURE SUMMARY

- NXP i.MX 8M Plus Family Processors.
 - ✓ 4x or 2x Cortex-A53 up to 1.8 GHz
 - ✓ Cortex-M7 up to 800 MHz
 - ✓ Neural Processing Unit (NPU): Delivers up to 2.3 TOPS.
 - ✓ Video Decode: 1080p60, h.265/4, VP9, VP8
 - ✓ Video Encode: 1080p60, h.265/ 4
 - ✓ GPU: 16 GFLOPS (high precision) OpenGL® ES 3.1/3.0, Vulkan®, Open CL™ 1.2 FP, OpenVG™ 1.1
- Up to 8GB of LPDDR4 SDRAM.
- Up to 128MB QSPI Flash(optional)
- Up to 128GB eMMC for boot/operating system/application/storage.
- 2x USB 3.0/2.0 Dual-Role with PHY type C
- Display: 4-Lane MIPI-DSI, HDMI 2.0a Tx, LVDS (4/8-lane) Tx
 - ✓ Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.
 - ✓ One LCDIF drives MIPI DSI, up to UWHD and WUXGA
 - ✓ One LCDIF drives LVDS Tx, up to 1920x1080p60.
 - ✓ One LCDIF drives HDMI Tx, up to 4kp30.
- Single Lane PCIe Gen 3
- Up to 2 x SAI
- Up to 4 x PDM
- Up to 1 x SPDIF

- Up to 2 x SDIO 3.0
- Up to 6 x I2C
- Up to 3 x SPI
- Up to 4 x UART
- Up to 2 x FlexCAN
- Up to 4 x PWM
- Two Instances of 4-Lane MIPI CSI
 - ✓ With one camera: support up to 12MP@30fps or 4kp45.
 - ✓ With two cameras: each supports up to 1080p80.
- GPIO
- High-Security Cryptographic Device IC (ATECC608, protected storage for up to 16 Keys, Certificates or Data) or On board I2C EEPROM.
- 1 x Gigabit Ethernet Controller
- On board 10/100/1000 Mbps Ethernet PHY
- On Board Audio Codec Supports Headphone Output, Microphone Input and Line Out
- On board 2.5GHz/5GHz WLAN (IEEE802.11 a/b/g/n), BT 4.2 and BLE module
- JTAG
- Single 5.0V Input Power Supply
- 4 bits Boot Mode DIP Switch (SW1) for selecting boot from either eMMC, Micro SD, QSPI Flash or serial download.
- 69.6mm x 40mm Form Factor
- 260 pin SO-DIMM DDR4 Interface

1.3 BLOCK DIAGRAM

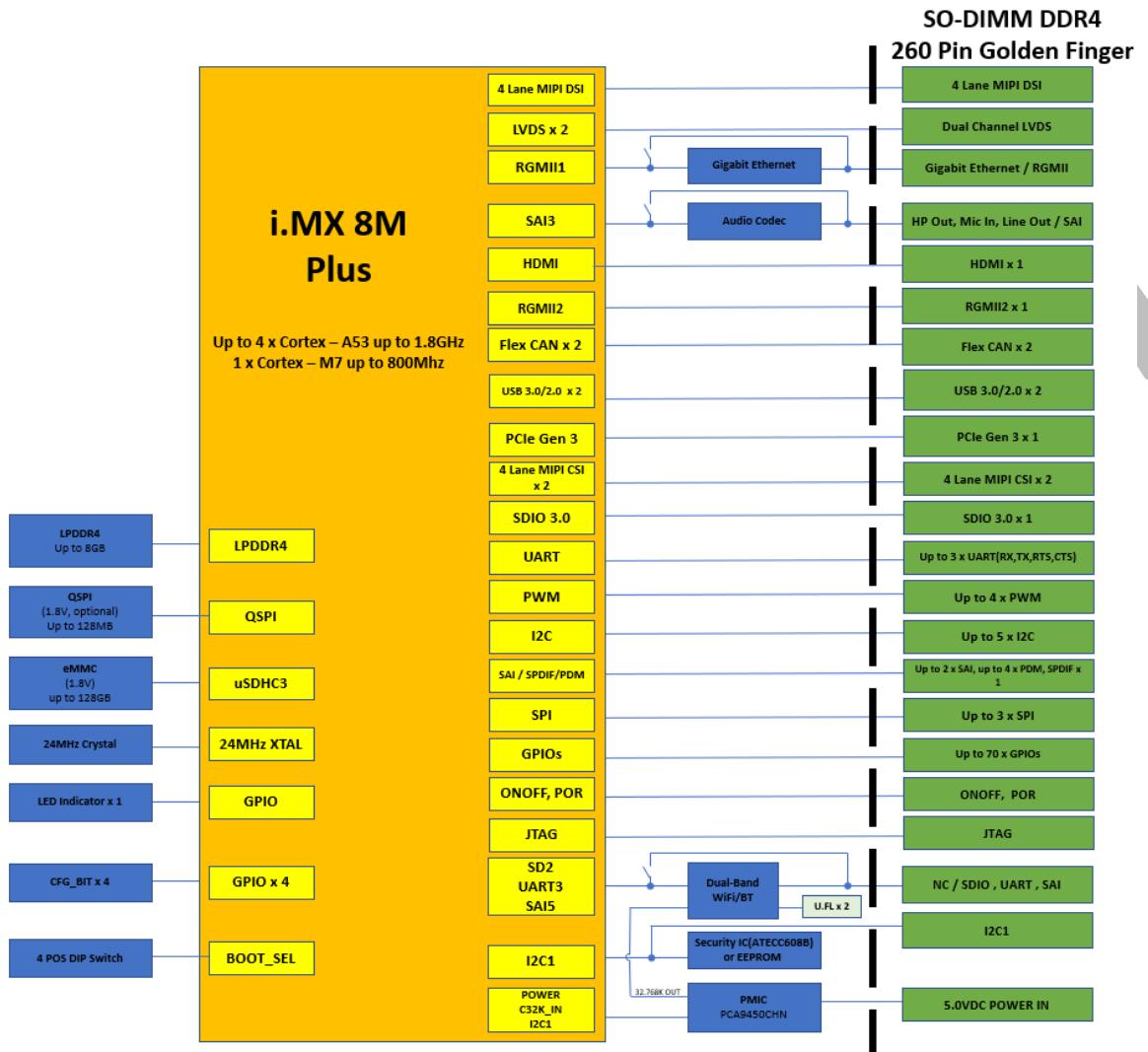


Figure 1-1: VEST i.MX8M Plus SOM Board Block diagram

1.4 VEST i.MX8M PLUS SOM BOARD, CONNECTORS AND DIP SWITCH LIST



Figure 1-2: VEST i.MX8M Plus SOM Board User Accessible Connector and Dip Switch List

The table below lists the user accessible connectors and dip switch on the VEST i.MX8M Plus SOM Board.

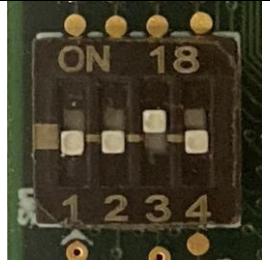
Reference	Function	Type	Pin 1 Location
CN2	2.4GHz U.FL RF Antenna Socket	U.FL	Standard
CN3	5GHz U.FL RF Antenna Socket	U.FL	Standard
D1	GPIO Controlled LED Indicator <i>iMX8M Plus Pad Name: NAND_READY_B</i>	Green	
SW1	Boot Mode Select Dip Switch	Vertical, 4 POS, 1.27mm pitch	

Table 1-2: VEST i.MX8M Plus SOM Board User Accessible Connector and Dip Switch List

2 MAIN HARDWARE COMPONENTS

This section summarizes the main SOM hardware building blocks.

2.1 NXP i.MX 8M Plus

2.1.1 Overview

The i.MX 8M Plus family focuses on machine learning, vision, advanced multimedia, and industrial automation with high reliability. It is built to meet the needs of Smart Home, Building, Smart City, and Industry 4.0 applications.

Powerful quad or dual Arm® Cortex®-A53 processor with a Neural Processing Unit (NPU) operating up to 2.3 TOPS.

Dual image signal processors (ISP) and two camera inputs for an advanced vision system.

The multimedia capabilities include video encode (including h.265) and decode, 3D/2D hardware graphic acceleration, and multiple audio and voice functions.

Real-time control with a Cortex-M7. Robust control networks supported by dual CAN FD and dual Gigabit Ethernet with Time Sensitive Networking (TSN).

High industrial reliability with DRAM inline ECC.

2.1.2 Features

Multicore Processing and Memory Interfaces

- 4x or 2x Cortex-A53 up to 1.8 GHz
- Cortex-M7 up to 800 MHz
- 32-bit DDR4 & LPDDR4 up to 4.0GT/s\

Machine Learning and Vision

- Neural Processing Unit (NPU) that delivers up to 2.3 TOPS.
- Dual Image Signal Processor (ISPs) with resolutions up to 12MP and input rate up to 375MPixels/s
- Camera Interface: 2x MIPI CSI

Advanced Multimedia and Display

- Video Decode: 1080p60, h.265/4, VP9, VP8
- Video Encode: 1080p60, h.265/4.
- GPU: 16 GFLOPS (high precision) OpenGL® ES 3.1/3.0, Vulkan®, Open CL™ 1.2 FP, OpenVG™ 1.1
- Audio: 18x I2S TDM, DSD512, S/PDIF Tx + Rx, 8-ch PDM Mic input, eARC, ASRC
- Low power voice accelerator: Cadence® Tensilica® HiFi 4 DSP @ 800 MHz
- Display: MIPI-DSI, HDMI 2.0a Tx, LVDS (4/8-lane) Tx

High Speed Interfaces

- 2x Gigabit Ethernet with AVB, IEEE 1588, EEE and 1x w/ TSN
- 2x USB 3.0/2.0 Dual-Role with PHY type C

- PCIe Gen 3
- 3x SDIO 3.0
- 2x CAN FD

Industrial Reliability

- DDR Inline ECC for LPDDR4 and DDR4
- 14 FinFET process with low soft error rate (SER)

Note:

1. Please to refer the latest i.MX8M Plus datasheet from NXP's website for details.

2.2 10/100/1000MBPS ETHERNET TRANSCEIVER

The SOM features a TI DP83867 single port Gigabit Ethernet PHY via RGMII interface to the MAC.

The DP83867 device is a low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T, 100BASE-TX, and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. It interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through Reduced GMII (RGMII) or embedded clock Serial GMII (SGMII).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

Designed for low power, the DP83867 consumes only 457 mW under full operating power. Wake-on-LAN can be used to further lower the system's power consumption.

The key features supported by the device are:

- Fully compatible with IEEE 802.3 10BASE-T, 100BASE-TX, and 1000BASE-T Specifications.
- Exceeds 8000 V IEC 61000-4-2 ESD protection.
- Meets EN55011 class B emission standards.
- 16 programmable RGMII delay modes on RX/TX
- Integrated MDI termination resistors
- Programmable MAC interface termination impedance
- WoL (Wake-on-LAN) packet detection
- 25-MHz or 125-MHz synchronized clock output
- Start of Frame Detect for IEEE 1588 timestamp.
- RJ45 mirror mode
- Cable diagnostics
- Fast link drop mode

2.3 MEMORY

2.3.1 LPDDR4 SDRAM

The SOM is available with up to 8GB of LPDDR4-4000 SDRAM.

Please see Section titled "[Board Options](#)" for the various memory options.

2.3.2 eMMC Flash Memory

The SOM is available with an eMMC Flash Memory with densities up to 128GB. The eMMC flash can be used for Flash Disk, O.S. run-time-image and the Boot-loader.

The eMMC is directly connected to i.MX8M Plus SDHC 3. The eMMC Flash memory is physically located on the top side of the SOM.

Please see Section titled "[Board Options](#)" for the various eMMC Flash options.

2.3.3 QSPI Flash Memory

The SOM can support up to 128MB QSPI Flash for Flash Disk, O.S. run-time-image and the bootloader.

The QSPI Flash by default is not mounted.

2.4 ON BOARD SECURITY IC OR I2C EEPROM

The SOM provides High-Security Cryptographic Device IC (ATECC608, with protected storage for up to 16 Keys, Certificates or Data) or on board I2C EEPROM, both share the same footprint and are directly connected to I2C1 bus.

ATECC608B Summary:

The Microchip ATECC608B integrates ECDH (Elliptic Curve Diffie Hellman) an ultra-secure security protocol to provide key agreement for encryption/decryption, along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication for the Internet of Things (IoT) market including home automation, industrial networking, medical, as well as accessories and consumables authentication and more. Additionally, the ATECC608B offer an integrated AES hardware accelerator strengthening hardware-based security for LoRaWAN applications and enable secure boot capabilities for very small microcontrollers.

Please see Section titled "[Board Options](#)" for the various options.

2.5 AUDIO CODEC

The SGTL5000 is a low-power stereo codec designed to provide a comprehensive audio solution for portable products that require line-in, mic-in, line-out, headphone-out, and digital I/O.

Feature:

- Ultra-low power with very high performance and functionality
- Capless headphone and an integrated PLL to allow clock reuse within the system and to achieve a lower overall system cost.
- MIC bias provided.

- Programmable MIC gain
- Auto volume control
- Line Out
- 100 dB SNR and -85 dB THD+N (VDDA=3.3 V)
- HP Output
- 98 dB SNR and -80 dB THD+N (VDDA=1.8 V 16 Ohm load, DAC to headphone)
- 45 mW max into 16 Ohm load @ 3.3 V
- Very good PSRR without Lin Reg.
- Ramped digital volumes.
- Popless volume
- 0.5 dB analog volume steps (0 dB to – 64 dB)

2.6 PMIC

The SOM uses a NXP PCA9450CHN Power Management IC. The PCA9450 is a single chip PMIC specifically designed to support i.MX 8M family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5 V adapter for nonportable applications.

The device provides six high-efficiency step-down regulators, five LDOs, one 400 mA load switch, 2 channel level translator, a 32.768 kHz crystal oscillator driver, and buck regulators. The buck regulators support dynamic voltage scaling (DVS) with programmable ramping up and down times and remote sensing to compensate for IR drop to the load.

2.7 ON BOARD WLAN AND BLUETOOTH MODULE

The SOM is configured with an WG7833-B0 wireless module from Jorjin technologies. The WG7833-B0 features a 2.4GHz / 5GHz dual band IEEE802.11 a/b/g/n/ac WLAN and Bluetooth 4.1 BR/EDR/LE (class 2) chipset from Qualcomm Atheros.

The Jorjin WG7833-B0 is a 2.4/5 GHz WLAN + Bluetooth system in a Sip package based on the WL1833 SoC from Texas Instruments.

It contains a crystal, power amplifier, Tx filter and Tx/Rx switch as well as the necessary passive components to fully implement the 802.11a, b, g, n Wi-Fi & Bluetooth 4.2 functions.

The WG7833-B0 WLAN is connected to the host processor via a 1.8V SDIO interface, and the Bluetooth is connected via a UART. Linux and Android drivers are provided for a wide range of application processors.

The SOM provides provisions for two 50 ohm U.FL (CN2 for 2.4GHz & CN3 for 5GHz) sockets for external dual band antennas.

[WG7833-B0 | Jorjin Technologies Inc. / A Pioneer of the AR Smart Glasses Industry](#)

2.8 BOARD SKU CONFIGURATION SETTINGS

Four GPIO bits are used internally, for different product SKU configuration settings. These GPIO bits are either pulled up or pulled down by 10k Ω resistors. These bits are:

Signal Name	i.MX8M Plus pad name	Signal	Signal Type	Voltage Level	Description
BOARD_CFG1	GPIO1_IO07	GPIO1_IO07	I	1.8V	Board configuration 1
BOARD_CFG2	GPIO1_IO08	GPIO1_IO08	I	1.8V	Board configuration 2
BOARD_CFG3	GPIO1_IO03	GPIO1_IO03	I	1.8V	Board configuration 3
BOARD_CFG4	GPIO1_IO06	GPIO1_IO06	I	1.8V	Board configuration 4

Table 2-1: Board SKU Configurations GPIO bits Settings

The BOARD SKU CONFIGURATION settings are:

Board Configuration Bit	Meaning
BOARD_CFG4	Reserved (default:0)
BOARD_CFG[3:1]	0 '000' -> Micron MT53D1024M32D4DT-046 WT:D

Table 2-2: The BOARD SKU configuration settings

3 EXTERNAL INTERFACE

The VEST i.MX8M Plus SOM employs a 260-pin DDR4 SO-DIMM standard interface. The recommended mating connector for interfacing is TE: 2309411-1 or equivalent.

Note:

The i.MX8M Plus contains a limited number of pins, most of which have multiple signal options that are muxed. These signal to pin and pin to signal options are selected by the input-output multiplexer called the IOMUX.

Below Pin assignments lists the pad names of the chip, the various signals that can be assigned to each of the pads, For more details please refer the latest i.MX8M Plus datasheet.

Pin Number.:	Pin number on the VEST i.MX8M Plus SOM edge connector
Pin Name:	Pin name on the VEST i.MX8M Plus SOM edge connector
i.MX8M Plus Pad Name:	Pad name on i.MX8M Plus
Signal Type:	Signal type of this pin
Voltage Level:	Voltage level of this pin
Description:	Brief pin functionality description

Table 3-1: VEST i.MX8M Plus SOM Golden Finger Pinout

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
1	NC or SD1_DATA3_1V8	SD1_DATA3		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
2	GND		Ground	0V	GND
3	NC or SD1_DATA2_1V8	SD1_DATA2		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
4	NC or PWM_4_1V8	SAI5_RXFS		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
5	NC or SD1_DATA1_1V8	SD1_DATA1		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
6	NC or BT_EN_1V8	SAI5_MCLK		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
7	NC or SD1_DATA0_1V8	SD1_DATA0		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
8	NC or WLAN IRQ_1V8	SAI1_RXC		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
9	NC or SD1_CMD_1V8	SD1_CMD		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
10	NC or WLAN_EN_1V8	SAI1_RXDO		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
11	NC or SD1_CLK_1V8	SD1_CLK		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
12	NC or SAI5_RXD_1V8	SAI5_RXD0		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
13	GND		Ground	0V	GND
14	NC or SAI5_TXD_1V8	SAI5_RXD3		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
15	ONOFF_1V8	ONOFF	Input (PU 100K)	1.8V	Power on/off
16	NC or SAI5_RXFS_1V8	SAI3_RXFS		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
17	SYS_nRST_1V8	PMIC pad PMIC_RST_B	Input	1.8V	PMIC Reset Input pin. It is internally pulled up to the PMIC LD01 Power rail. Once asserted, low, The PMIC performs a reset.
18	NC or SAI5_RXC_1V8	SAI3_RXC		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
19	SOM_PWR_GOOD_1V8	PMIC_ON_REQ	Output (PU 100K)	1.8V	SOM power good, active high
20	GND		Ground	0V	GND
21	NC or UART3_RTS_1V8	SD1_RESET_B		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
22	SD2_CLK	SD2_CLK		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	

Pin No.	Pin Name	<i>i</i> MX8M Plus Pad Name	Signal Type	Voltage Level	Description
23	NC or UART3_RXD_1V8	SD1_DATA7		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
24	SD2_CMD	SD2_CMD		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
25	NC or UART3_CTS_1V8	SD1_STROBE		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
26	SD2_DATA0	SD2_DATA0		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
27	NC or UART3_TXD_1V8	SD1_DATA6		1.8V	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
28	SD2_DATA1	SD2_DATA1		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
29	GND		Ground	0V	GND
30	SD2_DATA2	SD2_DATA2		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
31	LVDS0_TX3_N	LVDS0_D3_N	Differential		LVDS0 differential pair 3 negative
32	SD2_DATA3	SD2_DATA3		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
33	LVDS0_TX3_P	LVDS0_D3_P	Differential		LVDS0 differential pair 3 positive

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
34	<i>SD2_WP</i>	<i>SD2_WP</i>		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
35	<i>LVDS0_TX2_N</i>	<i>LVDS0_D2_N</i>	Differential		<i>LVDS0 differential pair 2 negative</i>
36	<i>SD2_nCD</i>	<i>SD2_CD_B</i>		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
37	<i>LVDS0_TX2_P</i>	<i>LVDS0_D2_P</i>	Differential		<i>LVDS0 differential pair 2 positive</i>
38	<i>SD2_RESET_B</i>	<i>SD2_RESET_B</i>		3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	
39	GND		Ground	0V	GND
40	GND		Ground	0V	GND
41	<i>LVDS0_CLK_N</i>	<i>LVDS0_CLK_N</i>	Differential		<i>LVDS0 clock differential pair negative</i>
42	<i>GPIO4_IO03_1V8</i>	<i>SAI1_RXD1</i>		1.8V	
43	<i>LVDS0_CLK_P</i>	<i>LVDS0_CLK_P</i>	Differential		<i>LVDS0 clock differential pair positive</i>
44	<i>GPIO4_IO21_1V8</i>	<i>SAI2_RXFS</i>		1.8V	
45	GND		Ground	0V	GND
46	<i>ECSPI1_SSO_1V8</i>	<i>ECSPI1_SSO</i>		1.8V	
47	<i>LVDS0_TX1_N</i>	<i>LVDS0_D1_N</i>	Differential		<i>LVDS0 differential pair 1 negative</i>
48	<i>ECSPI1_MOSI_1V8</i>	<i>ECSPI1_MOSI</i>		1.8V	
49	<i>LVDS0_TX1_P</i>	<i>LVDS0_D1_P</i>	Differential		<i>LVDS0 differential pair 1 positive</i>
50	<i>ECSPI1_MISO_1V8</i>	<i>ECSPI1_MISO</i>		1.8V	
51	<i>LVDS0_TX0_N</i>	<i>LVDS0_D0_N</i>	Differential		<i>LVDS0 differential pair 0 negative</i>
52	<i>ECSPI1_SCLK_1V8</i>	<i>ECSPI1_SCLK</i>		1.8V	
53	<i>LVDS0_TX0_P</i>	<i>LVDS0_D0_P</i>	Differential		<i>LVDS0 differential pair 0 positive</i>
54	GND		Ground	0V	GND
55	GND		Ground	0V	GND
56	<i>EARC_N_HPD</i>	<i>EARC_N_HPD</i>	Output	1.8V	
57	<i>LVDS1_TX3_N</i>	<i>LVDS1_D3_N</i>	Differential		<i>LVDS1 differential pair 3 negative</i>
58	<i>EARC_P_UTIL</i>	<i>EARC_P_UTIL</i>	Output	1.8V	
59	<i>LVDS1_TX3_P</i>	<i>LVDS1_D3_P</i>	Differential		<i>LVDS1 differential pair 3 positive</i>
60	<i>EARC_AUX</i>	<i>EARC_AUX</i>	Output	1.8V	
61	<i>LVDS1_TX2_N</i>	<i>LVDS1_D2_N</i>	Differential		<i>LVDS1 differential pair 2 negative</i>
62	<i>HDMI_HPD</i>	<i>HDMI_HPD</i>		1.8V	
63	<i>LVDS1_TX2_P</i>	<i>LVDS1_D2_P</i>	Differential		<i>LVDS1 differential pair 2 positive</i>
64	<i>HDMI_CEC</i>	<i>HDMI_CEC</i>		1.8V	
65	GND		Ground	0V	GND
66	GND		Ground	0V	GND

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
67	LVDS1_CLK_N	LVDS1_CLK_N	Differential		LVDS1 clock differential pair negative
68	HDMI_TX2_N	HDMI_TX2_N	Differential		HDMI differential data 2 negative
69	LVDS1_CLK_P	LVDS1_CLK_P	Differential		LVDS1 clock differential pair positive
70	HDMI_TX2_P	HDMI_TX2_P	Differential		HDMI differential data 2 positive
71	GND		Ground	0V	GND
72	HDMI_TX1_N	HDMI_TX1_N	Differential		HDMI differential data 1 negative
73	LVDS1_TX1_N	LVDS1_D1_N	Differential		LVDS1 differential pair 1 negative
74	HDMI_TX1_P	HDMI_TX1_P	Differential		HDMI differential data 1 positive
75	LVDS1_TX1_P	LVDS1_D1_P	Differential		LVDS1 differential pair 1 positive
76	GND		Ground	0V	GND
77	LVDS1_TX0_N	LVDS1_D0_N	Differential		HDMI differential data 0 negative
78	HDMI_TX0_N	HDMI_TX0_N	Differential		HDMI differential data 0 negative
79	LVDS1_TX0_P	LVDS1_D0_P	Differential		LVDS1 differential pair 0 positive
80	HDMI_TX0_P	HDMI_TX0_P	Differential		HDMI differential data 0 positive
81	GND		Ground	0V	GND
82	HDMI_TXC_N	HDMI_TXC_N	Differential		HDMI clock differential negative
83	CSI2_D0_N	MIPI_CSI2_D0_N	Differential		MIPI CSI2 differential pair 0 negative
84	HDMI_TXC_P	HDMI_TXC_P	Differential		HDMI clock differential positive
85	CSI2_D0_P	MIPI_CSI2_D0_P	Differential		MIPI CSI2 differential pair 0 positive
86	GND		Ground	0V	GND
87	CSI2_D1_N	MIPI_CSI2_D1_N	Differential		MIPI CSI2 differential pair 1 negative
88	HDMI_DDC_SCL	HDMI_DDC_SCL		1.8V	
89	CSI2_D1_P	MIPI_CSI2_D1_P	Differential		MIPI CSI2 differential pair 1 positive
90	HDMI_DDC_SDA	HDMI_DDC_SDA		1.8V	
91	GND		Ground	0V	GND
92	GPIO4_IO00_1V8	SAI1_RXFS		1.8V	
93	CSI2_CK_N	MIPI_CSI2_CLK_N	Differential		MIPI CSI2 clock differential pair negative
94	GPIO4_IO22_1V8	SAI2_RXC		1.8V	
95	CSI2_CK_P	MIPI_CSI2_CLK_P	Differential		MIPI CSI2 clock differential pair positive
96	GPIO3_IO22_1V8	SAI5_RXD1		1.8V	
97	GND		Ground	0V	GND
98	GPIO3_IO23_1V8	SAI5_RXD2		1.8V	
99	CSI2_D2_N	MIPI_CSI2_D2_N	Differential		MIPI CSI2 differential pair 2 negative
100	GPIO1_IO05_1V8	GPIO1_IO05		1.8V	
101	CSI2_D2_P	MIPI_CSI2_D2_P	Differential		MIPI CSI2 differential pair 2 positive
102	GND		Ground	0V	GND

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
103	CSI2_D3_N	MIPI_CSI2_D3_N	Differential		MIPI CSI2 differential pair 3 negative
104	CSI1_D3_P	MIPI_CSI1_D3_P	Differential		MIPI CSI1 differential pair 3 positive
105	CSI2_D3_P	MIPI_CSI2_D3_P	Differential		MIPI CSI2 differential pair 3 positive
106	CSI1_D3_N	MIPI_CSI1_D3_N	Differential		MIPI CSI1 differential pair 3 negative
107	GND		Ground	0V	GND
108	CSI1_D2_P	MIPI_CSI1_D2_P	Differential		MIPI CSI1 differential pair 2 positive
109	DSI_D3_N	MIPI_DSI1_D3_N	Differential		MIPI DSI differential pair 3 negative
110	CSI1_D2_N	MIPI_CSI1_D2_N	Differential		MIPI CSI1 differential pair 2 negative
111	DSI_D3_P	MIPI_DSI1_D3_P	Differential		MIPI DSI differential pair 3 positive
112	GND		Ground	0V	GND
113	DSI_D2_N	MIPI_DSI1_D2_N	Differential		MIPI DSI differential pair 2 negative
114	CSI1_CK_P	MIPI_CSI1_CLK_N	Differential		MIPI CSI1 clock differential pair negative
115	DSI_D2_P	MIPI_DSI1_D2_P	Differential		MIPI DSI differential pair 2 positive
116	CSI1_CK_N	MIPI_CSI1_CLK_P	Differential		MIPI CSI1 clock differential pair positive
117	GND		Ground	0V	GND
118	GND		Ground	0V	GND
119	DSI_CK_N	MIPI_DSI1_CLK_N	Differential		MIPI DSI clock differential negative
120	CSI1_D1_P	MIPI_CSI1_D1_P	Differential		MIPI CSI1 differential pair 1 positive
121	DSI_CK_P	MIPI_DSI1_CLK_P	Differential		MIPI DSI clock differential positive
122	CSI1_D1_N	MIPI_CSI1_D1_N	Differential		MIPI CSI1 differential pair 1 negative
123	GND		Ground	0V	GND
124	CSI1_D0_P	MIPI_CSI1_D0_P	Differential		MIPI CSI1 differential pair 0 negative
125	DSI_D1_N	MIPI_DSI1_D1_N	Differential		MIPI DSI differential pair 1 negative
126	CSI1_D0_N	MIPI_CSI1_D0_N	Differential		MIPI CSI1 differential pair 0 positive
127	DSI_D1_P	MIPI_DSI1_D1_P	Differential		MIPI DSI differential pair 1 positive
128	GND		Ground	0V	GND
129	DSI_D0_N	MIPI_DSI1_D0_N	Differential		MIPI DSI differential pair 0 negative
130	CSI_MCLK_1V8	GPIO1_IO15		1.8V	
131	DSI_D0_P	MIPI_DSI1_D0_P	Differential		MIPI DSI differential pair 0 positive
132	USB1_EN_1V8	GPIO1_IO12		1.8V	
133	GND		Ground	0V	GND
134	USB1_OC_1V8	GPIO1_IO13		1.8V	
135	PCIE_TX_N	PCIE_TXN_N	Differential		PCIe differential transmit negative
136	USB1_VBUS_3V3	USB1_VBUS	Input		USB1 PHY VBUS
137	PCIE_TX_P	PCIE_TXN_P	Differential		PCIe differential transmit positive

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
138	USB1_ID_1V8	GPIO1_IO10		1.8V	
139	PCIE_RX_N	PCIE_RXN_N	Differential		PCIe differential receive negative
140	USB1_D_N	USB1_D_N	Differential		USB1 PHY data negative
141	PCIE_RX_P	PCIE_RXN_P	Differential		PCIe differential receive positive
142	USB1_D_P	USB1_D_P	Differential		USB1 PHY data positive
143	GND		Ground	0V	GND
144	GND		Ground	0V	GND
145	PCIE_CLK_N	PCIE_REF_PAD_CLK_N	Differential		PCIe clock differential negative
146	GND		Ground	0V	GND
147	PCIE_CLK_P	PCIE_REF_PAD_CLK_P	Differential		PCIe clock differential positive
148	SAI2_MCLK_1V8	SAI2_MCLK	Ground	0V	GND
149	GND		Ground	0V	GND
150	SAI2_TXFS_1V8	SAI2_TXFS		1.8V	
151	USB2_TX_N	USB2_TX_N	Differential		USB2 PHY 3.0 transmit data negative
152	SAI2_TXD_1V8	SAI2_TXDO		1.8V	
153	USB2_TX_P	USB2_TX_P	Differential		USB2 PHY 3.0 transmit data positive
154	SAI2_RXD_1V8	SAI2_RXDO		1.8V	
155	USB2_RX_N	USB2_RX_N	Differential		USB2 PHY 3.0 receive data negative
156	SAI2_TXC_1V8	SAI2_TXC		1.8V	
157	USB2_RX_P	USB2_RX_P	Differential		USB2 PHY 3.0 receive data positive
158	GND		Ground	0V	GND
159	GND		Ground	0V	GND
160	JTAG_TDI_1V8	JTAG_TDI		1.8V	JTAG TDI
161	USB1_TX_N	USB1_TX_N	Differential		USB2 PHY 3.0 transmit data negative
162	JTAG_TDO_1V8	JTAG_TDO		1.8V	JTAG TDO
163	USB1_TX_P	USB1_TX_P	Differential		USB2 PHY 3.0 transmit data positive
164	JTAG_TMS_1V8	JTAG_TMS		1.8V	JTAG TMS
165	USB1_RX_N	USB1_RX_N	Differential		USB2 PHY 3.0 receive data negative
166	JTAG_TCK_1V8	JTAG_TCK		1.8V	JTAG TCK
167	USB1_RX_P	USB1_RX_P	Differential		USB2 PHY 3.0 receive data positive
168	JTAG_MOD_1V8	JTAG_MOD		1.8V	JTAG MODE
169	GND		Ground	0V	GND
170	GPIO4_IO20_1V8	SAI1_MCLK		1.8V	
171	USB2_D_N	USB2_D_N	Differential		USB2 PHY data negative
172	GND		Ground	0V	GND
173	USB2_D_P	USB2_D_P	Differential		USB2 PHY data positive
174	UART4_RXD_1V8	ECSPI2_SCLK		1.8V	
175	USB2_EN_1V8	GPIO1_IO14		1.8V	
176	UART4_TXD_1V8	ECSPI2_MOSI		1.8V	
177	USB2_VBUS_3V3	USB2_VBUS	Input		USB2 PHY VBUS
178	UART4_RTS_1V8	ECSPI2_SSO		1.8V	
179	USB2_ID_1V8	GPIO1_IO11		1.8V	
180	UART4_CTS_1V8	ECSPI2_MISO		1.8V	
181	GND		Ground	0V	GND
182	CAN1_TX_1V8	SPDIF_TX		1.8V	

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
183	POR_B_1V8	POR_B	Input (PU 100K)	1.8V	Reset the entire chip
184	CAN1_RX_1V8	SPDIF_RX		1.8V	
185	I2C1_SCL_1V8	I2C1_SCL	Output	1.8V	I2C1 SCL
186	CAN2_TX_1V8	UART3_RXD		1.8V	
187	I2C1_SDA_1V8	I2C1_SDA	I/O	1.8V	I2C1 SDA
188	CAN2_RX_1V8	UART3_TXD		1.8V	
189	HP_DETECT_1V8	GPIO1_IO01		1.8V	
190	GND		Ground	0V	GND
191	GND		Ground	0V	GND
192	UART1_RXD_1V8	UART1_RXD		1.8V	
193	PWM_3_1V8	SAI5_RXC		1.8V	
194	UART1_TXD_1V8	UART1_TXD		1.8V	
195	PWM_1_1V8	SPDIF_EXT_CLK		1.8V	
196	UART2_RTS_1V8	UART4_RXD		1.8V	
197	PWM_2_1V8	GPIO1_IO09		1.8V	
198	UART2_CTS_1V8	UART4_RXD		1.8V	
199	GND		Ground	0V	GND
200	UART2_RXD_1V8	UART2_RXD		1.8V	
201	I2C4_SCL_1V8	I2C4_SCL		1.8V	
202	UART2_TXD_1V8	UART2_TXD		1.8V	
203	I2C4_SDA_1V8	I2C4_SDA		1.8V	
204	GND		Ground	0V	GND
205	I2C2_SCL_1V8	I2C2_SCL		1.8V	
206	LINE_OUTR	Codec LINEOUT_R			SKUs with an Audio Codec
	SAI3_TXC_SOM_1V8	SAI3_TXC			SKUs without an Audio Codec
207	I2C2_SDA_1V8	I2C2_SDA		1.8V	
208	LINE_OUTL	Codec LINEOUT_L			SKUs with an Audio Codec
	SAI3_TXFS_SOM_1V8	SAI3_TXFS			Variants without an Audio Codec
209	I2C3_SCL_1V8	I2C3_SCL		1.8V	
210	HP_L	Codec HP_L			SKUs with an Audio Codec
	SAI3_RXD_SOM_1V8	SAI3_RXD			SKUs without an Audio Codec
211	I2C3_SDA_1V8	I2C3_SDA		1.8V	
212	HP_R	Codec HP_R			SKUs with an Audio Codec
	SAI3_TXD_SOM_1V8	SAI3_TXD			SKUs without an Audio Codec
213	GND		Ground	0V	GND
214	MIC_IN	Codec MIC			SKUs with an Audio Codec
	SAI3_MCLK_SOM_1V8	SAI3_MCLK		1.8V	SKUs without an Audio Codec
215	ENET_nRST_1V8	SD1_DATA4		1.8V	
216	GND		Ground	0V	GND
217	ETH1_LED_ACT	Ethernet PHY LED_2		1.8V	For SKUs with on-board Ethernet PHY LED output for 10/100/1000Base-T activity, active high
	ENET_nINT_1V8	SD1_DATA5		1.8V	SKUs without an on-board Ethernet PHY
218	ENET2_RGMII_nINT_1V8	SAI1_TXD6		1.8V	

Pin No.	Pin Name	<i>i</i> MX8M Plus Pad Name	Signal Type	Voltage Level	Description
219	ETH1_LED_10_100	Ethernet PHY LED_0		1.8V	For SKUs with on-board Ethernet PHY LED output for 10/100Base-T link, active high
	ENET_MIDO_1V8	ENET_MDIO		1.8V	SKUs without an on-board Ethernet PHY
220	ENET2_RGMII_MDIO_1V8	SAI1_RXD3		1.8V	
221	ETH1_LED_1000	Ethernet PHY LED_1		1.8V	SKUs with on-board Ethernet PHY LED output for 1000Base-T link, active high
	ENET_MDC_1V8	ENET_MDC		1.8V	SKUs without an on-board Ethernet PHY
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2		1.8V	
223	NC or ENET_RX_CTL_SOM_1V8	ENET_RX_CTL		1.8V	SKUs without an on-board Ethernet PHY
224	GND		Ground	0V	GND
225	NC or ENET_RXC_SOM_1V8	ENET_RXC		1.8V	SKUs without an on-board Ethernet PHY
226	ENET2_RGMII_RXC_1V8	SAI1_TXC		1.8V	
227	GND		Ground	0V	GND
228	ENET2_RGMII_RX_CTL_1V8	SAI1_TXFS		1.8V	
229	ETH1_TRXO_P				SKUs with on-board Ethernet PHY Media-dependent interface 0, differential 100Ω transmission line
	ENET_RDO_SOM_1V8	ENET_RDO		1.8V	SKUs without an on-board Ethernet PHY
230	ENET2_RGMII_RDO_1V8	SAI1_RXD4		1.8V	
231	ETH1_TRXO_N				SKUs with on-board Ethernet PHY Media-dependent interface 0, differential 100Ω transmission line
	ENET_RD1_SOM_1V8	ENET_RD1		1.8V	SKUs without an on-board Ethernet PHY
232	ENET2_RGMII_RD1_1V8	SAI1_RXD5		1.8V	
233	GND		Ground	0V	SKUs with on-board Ethernet PHY GND
	ENET_RD2_SOM_1V8	ENET_RD2		1.8V	SKUs with an on-board Ethernet PHY GND
234	ENET2_RGMII_RD2_1V8	SAI1_RXD6		1.8V	
235	ETH1_TRX1_P				SKUs with on-board Ethernet PHY Media-dependent interface 1, differential 100Ω transmission line
	ENET_RX3_SOM_1V8	ENET_RX3		1.8V	SKUs without an on-board Ethernet PHY
236	ENET2_RGMII_RD3_1V8	SAI1_RXD7		1.8V	
237	ETH1_TRX1_N				SKUs with on-board Ethernet PHY Media-dependent interface 1, differential 100Ω transmission line

Pin No.	Pin Name	iMX8M Plus Pad Name	Signal Type	Voltage Level	Description
	<i>ENET_TXC_SOM_1V8</i>	<i>ENET_TXC</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
238	<i>GND</i>		<i>Ground</i>	0V	<i>GND</i>
239	<i>GND</i>		<i>Ground</i>	0V	<i>GND</i>
240	<i>ENET2_RGMII_TXC_1V8</i>	<i>SAI1_TXD5</i>		1.8V	
241	<i>ETH1_TRX2_P</i>				<i>SKUs with on-board Ethernet PHY Media-dependent interface 2, differential 100Ω transmission line</i>
	<i>ENET_TX_CTL_SOM_1V8</i>	<i>ENET_TX_CTL</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
242	<i>ENET2_RGMII_TX_CTL_1V8</i>	<i>SAI1_TXD4</i>		1.8V	
243	<i>ETH1_TRX2_N</i>				<i>SKUs with on-board Ethernet PHY Media-dependent interface 2, differential 100Ω transmission line</i>
	<i>ENET_TD0_SOM_1V8</i>	<i>ENET_TDO</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
244	<i>ENET2_RGMII_TD0_1V8</i>	<i>SAI1_TXD0</i>		1.8V	
245	<i>GND</i>		<i>Ground</i>		<i>SKUs with on-board Ethernet PHY GND</i>
	<i>ENET_TD1_SOM_1V8</i>	<i>ENET_TD1</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
246	<i>ENET2_RGMII_TD1_1V8</i>	<i>SAI1_TXD1</i>		1.8V	
247	<i>ETH1_TRX3_P</i>				<i>SKUs with on-board Ethernet PHY Media-dependent interface 3, differential 100Ω transmission line</i>
	<i>ENET_TD2_SOM_1V8</i>	<i>ENET_TD2</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
248	<i>ENET2_RGMII_TD2_1V8</i>	<i>SAI1_TXD2</i>		1.8V	
249	<i>ETH1_TRX3_N</i>				<i>SKUs with on-board Ethernet PHY Media-dependent interface 3, differential 100Ω transmission line</i>
	<i>ENET_TD3_SOM_1V8</i>	<i>ENET_TD3</i>		1.8V	<i>SKUs without an on-board Ethernet PHY</i>
250	<i>ENET2_RGMII_TD3_1V8</i>	<i>SAI1_TXD3</i>		1.8V	
251	<i>GND</i>		<i>Ground</i>	0V	<i>GND</i>
252	<i>GND</i>		<i>Ground</i>	0V	<i>GND</i>
253	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
254	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
255	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
256	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
257	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
258	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
259	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>
260	<i>SOM_5V0</i>		<i>Power</i>	5.0V	<i>5.0V Power Input</i>

4 VEST i.MX8M PLUS SOM CONNECTOR PIN MUX

The i.MX8M Plus has a limited number of pins, so many of the pins are muxed to provide more functionality. These signal to pin and pin to signal options are selected by the IOMUX.

The table below shows the Mux Pin assignments, the pad names of the chip, the various signals that can be assigned to each of the pads. For more detail please refer the latest i.MX8M Plus datasheet.

Table 4-1: VEST i.MX8M Plus SOM Connector Pin Mux

Pin No.	VEST i.MX8M Plus SOM Pin Name	i.MX8M Plus Pad Name	GPIO	SAI	USDHCI	I2C	UART	ENET1	ECSPI	USB	PWM	FLEXCAN	HDMI	CCM	SPDIF	PCIE	
1	SD1_DATA3_1V8	SD1_DATA3	GPIO2_I_05		USDHCI1_DATA3	I2C4_SDA	UART2_R_X	ENET1_R_GMII_RD_1									
3	SD1_DATA2_1V8	SD1_DATA2	GPIO2_I_04		USDHCI1_DATA2	I2C4_SCL	UART2_T_X	ENET1_R_GMII_RD_0									
4	PWM_4_1V8	SAI5_RXFS	GPIO3_I_O19	SAI5_RX_SYNC SAI1_TX_DATA0		I2C6_SCL					PWM4_O_UT						
5	SD1_DATA1_1V8	SD1_DATA1	GPIO2_I_03		USDHCI1_DATA1	I2C6_SDA	UART1_C_TS_B	ENET1_R_GMII_TD_0									
6	BT_EN_1V8	SAI5_MCLK	GPIO3_I_O25	SAI5_MC_LK SAI1_TX_BCLK		I2C5_SDA					PWM1_O_UT	CAN2_RX					
7	SD1_DATA0_1V8	SD1_DATA0	GPIO2_I_02		USDHCI1_DATA0	I2C6_SCL	UART1_R_TS_B	ENET1_R_GMII_TD_1									
8	WLAN IRQ_1V8	SAI1_RXC	GPIO4_I_01	SAI1_RX_BCLK													
9	SD1_CMD_1V8	SD1_CMD	GPIO2_I_01		USDHCI1_CMD	I2C5_SDA	UART1_R_X	ENET1_MDIO									
10	WLAN_EN_1V8	SAI1_RXDO	GPIO4_I_02	SAI1_RX_DATA0 SAI1_TX_DATA1													
11	SD1_CLK_1V8	SD1_CLK	GPIO2_I_00		USDHCI1_CLK	I2C5_SCL	UART1_T_X	ENET1_MDC									
12	SAI5_RXD_1V8	SAI5_RXDO	GPIO3_I_O21	SAI5_RX_DATA SAI1_TX_DATA2		I2C5_SCL					PWM2_O_UT						
14	SAI5_TXD_1V8	SAI5_RXD3	GPIO3_I_O24	SAI5_RX_DATA3 SAI1_TX_DATA5 SAI1_RX_SYNC SAI5_RX_DATA0								CAN2_TX					
16	SAI5_RXFS_1V8	SAI3_RXFS	GPIO4_I_O28	SAI3_RX_SYNC SAI2_RX_DATA1 SAI5_RX_SYNC SAI3_RX_DATA1										SPDIF1_IN			
18	SAI5_RXC_1V8	SAI3_RXC	GPIO4_I_O29	SAI3_RX_BCLK SAI2_RX_DATA2 SAI5_RX_BCLK			UART2_C_TS_B										
21	UART3 RTS_1V8	SD1_RESET_B	GPIO2_I_010		USDHCI1_RESET_B	I2C3_SCL	UART3_R_TS_B	ENET1_T_X_CLK									
22	SD2_CLK	SD2_CLK	GPIO2_I_013		USDHCI2_CLK		UART4_R_X		ECSPI2_S_CLK								
23	UART3_RXD_1V8	SD1_DATA7	GPIO2_I_09		USDHCI1_DATA7	I2C2_SDA	UART3_R_X	ENET1_R_X_ER									
24	SD2_CMD	SD2_CMD	GPIO2_I_014		USDHCI2_CMD		UART4_T_X		ECSPI2_MOSI								
25	UART3_CTS_1V8	SD1_STROBE	GPIO2_I_011		USDHCI1_STROBE	I2C3_SDA	UART3_C_TS_B										
26	SD2_DATA0	SD2_DATA0	GPIO2_I_015		USDHCI2_DATA0	I2C4_SDA	UART2_R_X										
27	UART3_TXD_1V8	SD1_DATA6	GPIO2_I_08		USDHCI1_DATA6	I2C2_SCL	UART3_T_X	ENET1_R_GMII_RX_CTL									
28	SD2_DATA1	SD2_DATA1	GPIO2_I_016		USDHCI2_DATA1	I2C4_SCL	UART2_T_X										
30	SD2_DATA2	SD2_DATA2	GPIO2_I_017		USDHCI2_DATA2				ECSPI2_S_SO						SPDIF1_O_UT		
32	SD2_DATA3	SD2_DATA3	GPIO2_I_018		USDHCI2_DATA3				ECSPI2_MISO						SPDIF1_IN		
34	SD2_WP	SD2_WP	GPIO2_I_020		USDHCI2_WP												

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	GPIO	SAI	USDHC	I2C	UART	ENET1	ECSPI	USB	PWM	FLEXCAN	HDMI	CCM	SPDIF	PCIE
36	SD2_nCD	SD2_CD_B	GPIO2_I_012		USDHC2_CD_B											
38	SD2_RESET_B	SD2_RESET_B	GPIO2_I_019		USDHC2_RESET_B											
42	GPIO4_IO03_1V8	SAI1_RXD1	GPIO4_I_03	SAI1_RX_DATA1												
44	GPIO4_IO21_1V8	SAI2_RXFS	GPIO4_I_021	SAI2_RX_SYNC SAI5_TX_SYNC SAI5_TX_DATA1 SAI2_RX_DATA1			UART1_T_X									
46	ECSPI1_SS0_1V8	ECSPI1_SS0	GPIO5_I_09	SAI7_TX_SYNC		I2C2_SDA	UART3_R_TS_B		ECSPI1_SS0							
48	ECSPI1_MOSI_1V8	ECSPI1_MOSI	GPIO5_I_07	SAI7_RX_BCLK			UART3_T_X		ECSPI1_MOSI							
50	ECSPI1_MISO_1V8	ECSPI1_MISO	GPIO5_I_08	SAI7_RX_DATA0		I2C2_SCL	UART3_C_TS_B		ECSPI1_MISO							
52	ECSPI1_SCLK_1V8	ECSPI1_SCLK	GPIO5_I_06	SAI7_RX_SYNC			UART3_R_X		ECSPI1_SCLK							
62	HDMI_HPD	HDMI_HPD	GPIO3_I_029			I2C6_SDA					CAN2_RX	HDMI_HPD/HDMI_HPD_O				
64	HDMI_CEC	HDMI_CEC	GPIO3_I_028			I2C6_SCL					CAN2_TX	HDMI_CEC				
88	HDMI_DDC_SCL	HDMI_DDC_SCL	GPIO3_I_026			I2C5_SCL					CAN1_TX	HDMI_SC_L				
90	HDMI_DDC_SDA	HDMI_DDC_SDA	GPIO3_I_027			I2C5_SDA					CAN1_RX	HDMI_SD_A				
92	GPIO4_IO00_1V8	SAI1_RXFS	GPIO4_I_00	SAI1_RX_SYNC												
94	GPIO4_IO22_1V8	SAI2_RXC	GPIO4_I_022	SAI2_RX_BCLK SAI5_TX_BCLK			UART1_R_X				CAN1_TX					
96	GPIO3_IO22_1V8	SAI5_RXD1	GPIO3_I_022	SAI5_RX_DATA1 SAI1_TX_DATA1 SAI1_TX_SYNC SAI5_TX_SYNC							CAN1_TX					
98	GPIO3_IO23_1V8	SAI5_RXD2	GPIO3_I_023	SAI5_RX_DATA2 SAI1_TX_DATA4 SAI1_TX_SYNC SAI5_TX_BCLK							CAN1_RX					
100	GPIO1_IO05_1V8	GPIO1_IO05	GPIO1_I_05											CCM_PM_IC_READ_Y		
130	CSI_MCLK_1V8	GPIO1_IO15	GPIO1_I_015		USDHC3_WP					USB2_OC	PWM4_O_UT			CCM_CLK_O2		
132	USB1_EN_1V8	GPIO1_IO12	GPIO1_I_012							USB1_P_WR						
134	USB1_OC_1V8	GPIO1_IO13	GPIO1_I_013							USB1_OC	PWM2_O_UT					
138	USB1_ID_1V8	GPIO1_IO10	GPIO1_I_010							USB1_ID	PWM3_O_UT					
148	SAI2_MCLK_1V8	SAI2_MCLK	GPIO4_I_027	SAI2_MC_LK SAI5_MC_LK SAI9_MC_LK								CAN2_RX				
150	SAI2_TXFS_1V8	SAI2_TXFS	GPIO4_I_024	SAI2_TX_SYNC SAI5_TX_DATA1 SAI2_TX_DATA1			UART1_C_TS_B									
152	SAI2_TXD_1V8	SAI2_TXD0	GPIO4_I_026	SAI2_TX_DATA0 SAI5_TX_DATA3								CAN2_TX				
154	SAI2_RXD_1V8	SAI2_RXD0	GPIO4_I_023	SAI2_RX_DATA0 SAI5_TX_DATA0 SAI2_TX_DATA1				UART1_R_TS_B								
156	SAI2_TC_1V8	SAI2_TC	GPIO4_I_025	SAI2_TX_BCLK SAI5_TX_DATA2								CAN1_RX				
170	GPIO4_IO20_1V8	SAI1_MCLK	GPIO4_I_020	SAI1_MC_LK SAI1_TX_BCLK				ENET1_T_X_CLK								
174	UART4_RXD_1V8	ECSPI2_SCLK	GPIO5_I_010	SAI7_TX_BCLK		I2C3_SCL	UART4_R_X		ECSPI2_SCLK							
175	USB2_EN_1V8	GPIO1_IO14	GPIO1_I_014		USDHC3_CD_B					USB2_P_WR	PWM3_O_UT			CCM_CLK_O1		
176	UART4_TXD_1V8	ECSPI2_MOSI	GPIO5_I_011	SAI7_TX_DATA0		I2C3_SDA	UART4_T_X		ECSPI2_MOSI							
178	UART4 RTS_1V8	ECSPI2_SS0	GPIO5_I_013			I2C4_SDA	UART4_R_TS_B		ECSPI2_SS0					CCM_CLK_O2		

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	GPIO	SAI	USDHC	I2C	UART	ENET1	ECSPI	USB	PWM	FLEXCAN	HDMI	CCM	SPDIF	PCIE
179	USB2_ID_1V8	GPIO1_IO11	GPIO1_I_O11		USDHC3_VSELECT					USB2_ID	PWM2_UT			CCM_PM_IC_READ_Y		
180	UART4_CTS_1V8	ECSPI2_MISO	GPIO5_I_O12	SAI7_MC_LK		I2C4_SCL	UART4_C_TS_B		ECSPI2_MISO					CCM_CLK_O1		
182	CAN1_TX_1V8	SPDIF_TX	GPIO5_I_O3			I2C5_SCL					PWM3_UT	CAN1_TX			SPDIF1_O_UT	
184	CAN1_RX_1V8	SPDIF_RX	GPIO5_I_O4			I2C5_SDA					PWM2_UT	CAN1_RX			SPDIF1_IN	
186	CAN2_TX_1V8	UART3_RXD	GPIO5_I_O26		USDHC3_RESET_B		UART3_R_X_UART1_C_TS_B					CAN2_TX				
188	CAN2_RX_1V8	UART3_TXD	GPIO5_I_O27		USDHC3_VSELECT		UART3_T_X_UART1_R_TS_B					CAN2_RX				
189	HP_DETECT_1V8	GPIO1_IO01	GPIO1_I_O1								PWM1_UT			CCM_REF_CLK_24_M_CCM_EXT_CLK2		
192	UART1_RXD_1V8	UART1_RXD	GPIO5_I_O22				UART1_R_X		ECSPI3_S_CLK							
193	PWM_3_1V8	SAI5_RXC	GPIO3_I_O20	SAI5_RX_BCLK_SAI1_TX_DATA1		I2C6_SDA					PWM3_UT					
194	UART1_TXD_1V8	UART1_TXD	GPIO5_I_O23				UART1_T_X		ECSPI3_MOSI							
195	PWM_1_1V8	SPDIF_EXT_CLK	GPIO5_I_O5								PWM1_UT				SPDIF1_E_XT_CLK	
196	UART2 RTS_1V8	UART4_TXD	GPIO5_I_O29			I2C6_SDA	UART4_T_X_UART2_R_TS_B									
197	PWM_2_1V8	GPIO1_IO09	GPIO1_I_O9		USDHC3_RESET_B						PWM2_UT					
198	UART2_CTS_1V8	UART4_RXD	GPIO5_I_O28			I2C6_SCL	UART4_R_X_UART2_C_TS_B									PCIE1_CL_KREQ_B
200	UART2_RXD_1V8	UART2_RXD	GPIO5_I_O24				UART2_R_X		ECSPI3_MISO							
201	I2C4_SCL_1V8	I2C4_SCL	GPIO5_I_O20			I2C4_SCL			ECSPI2_MISO		PWM2_UT					PCIE1_CL_KREQ_B
202	UART2_TXD_1V8	UART2_TXD	GPIO5_I_O25				UART2_T_X		ECSPI3_S_SO							
203	I2C4_SDA_1V8	I2C4_SDA	GPIO5_I_O21			I2C4_SDA			ECSPI2_S_SO		PWM1_UT					
205	I2C2_SCL_1V8	I2C2_SCL	GPIO5_I_O16		USDHC3_CD_B	I2C2_SCL			ECSPI1_MISO							
206	SAI3_TXC_SOM_1V8	SAI3_TXC	GPIO5_I_O0	SAI3_TX_BCLK_SAI2_TX_DATA2_SAI5_RX_DATA2			UART2_T_X									
207	I2C2_SDA_1V8	I2C2_SDA	GPIO5_I_O17		USDHC3_WP	I2C2_SDA			ECSPI1_S_SO							
208	SAI3_TXFS_SOM_1V8	SAI3_TXFS	GPIO4_I_O31	SAI3_TX_SYNC_SAI2_TX_DATA1_SAI5_RX_DATA1_SAI3_TX_DATA1				UART2_R_X								
209	I2C3_SCL_1V8	I2C3_SCL	GPIO5_I_O18			I2C3_SCL			ECSPI2_S_CLK		PWM4_UT					
210	SAI3_RXD_SOM_1V8	SAI3_RXD	GPIO4_I_O30	SAI3_RX_DATA0_SAI2_RX_DATA3_SAI5_RX_DATA0				UART2_R_TS_B								
211	I2C3_SDA_1V8	I2C3_SDA	GPIO5_I_O19			I2C3_SDA			ECSPI2_MOSI		PWM3_UT					
212	SAI3_TDX_SOM_1V8	SAI3_TDX	GPIO5_I_O1	SAI3_TX_DATA0_SAI2_TX_DATA3_SAI5_RX_DATA3											SPDIF1_E_XT_CLK	
214	SAI3_MCLK_SOM_1V8	SAI3_MCLK	GPIO5_I_O2	SAI3_MC_LK_SAI5_MC_LK							PWM4_UT				SPDIF1_O_UT_SPDIF1_IN	
215	ENET_nRST_1V8	SD1_DATA4	GPIO2_I_O6		USDHC1_DATA4	I2C1_SCL	UART2_R_TS_B	ENET1_R_GMII_TX_CTL								
217	ENET_nINT_1V8	SD1_DATA5	GPIO2_I_O7		USDHC1_DATA5	I2C1_SDA	UART2_C_TS_B	ENET1_T_X_ER								
218	ENET2_RGMII_nINT_1V8	SAI1_TDX6	GPIO4_I_O18	SAI1_RX_SYNC_SAI6_RX_SYNC_SAI6_TX_SYNC												
219	ENET_MIDO_1V8	ENET_MDIO	GPIO1_I_O17	SAI6_TX_SYNC	USDHC3_DATA5											

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	GPIO	SAI	USDHC	I2C	UART	ENET1	ECSPI	USB	PWM	FLEXCAN	HDMI	CCM	SPDIF	PCIE
220	ENET2_RGMII_MDIO_1V8	SAI1_RXD3	GPIO4_I05	SAI1_RX_DATA3				ENET1_MDIO								
221	ENET_MDC_1V8	ENET_MDC	GPIO1_I016	SAI6_TX_DATA0	USDHC3_STROBE											
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2	GPIO4_I04	SAI1_RX_DATA2				ENET1_MDC								
223	ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	GPIO1_I024	SAI7_TX_SYNC	USDHC3_DATA2											
225	ENET_RXC_SOM_1V8	ENET_RXC	GPIO1_I025	SAI7_TX_BCLK	USDHC3_DATA3											
226	ENET2_RGMII_RXC_1V8	SAI1_TXC	GPIO4_I011	SAI1_RX_BCLK				ENET1_R_GMII_RX_C								
228	ENET2_RGMII_RX_CTL_1V8	SAI1_TXFS	GPIO4_I010	SAI1_RX_SYNC				ENET1_R_GMII_RX_CTL								
229	ENET_RDO_SOM_1V8	ENET_RDO	GPIO1_I026	SAI7_RX_DATA0	USDHC3_DATA4											
230	ENET2_RGMII_RDO_1V8	SAI1_RXD4	GPIO4_I06	SAI1_RX_DATA4 SAI6_TX_BCLK SAI6_RX_BCLK				ENET1_R_GMII_RD0								
231	ENET_RD1_SOM_1V8	ENET_RD1	GPIO1_I027	SAI7_RX_SYNC	USDHC3_RESET_B											
232	ENET2_RGMII_RD1_1V8	SAI1_RXD5	GPIO4_I07	SAI1_RX_DATA5 SAI6_TX_DATA0 SAI6_RX_DATA0 SAI1_RX_SYNC				ENET1_R_GMII_RD1								
233	ENET_RD2_SOM_1V8	ENET_RD2	GPIO1_I028	SAI7_RX_BCLK	USDHC3_CLK											
234	ENET2_RGMII_RD2_1V8	SAI1_RXD6	GPIO4_I08	SAI1_RX_DATA6 SAI6_TX_SYNC SAI6_RX_SYNC				ENET1_R_GMII_RD2								
235	ENET_RX3_SOM_1V8	ENET_RX3	GPIO1_I029	SAI7_MC_LK	USDHC3_CMD										SPDIF1_IN	
236	ENET2_RGMII_RD3_1V8	SAI1_RXD7	GPIO4_I09	SAI1_RX_DATA7 SAI6_MC_LK SAI1_RX_SYNC SAI1_TX_DATA4				ENET1_R_GMII_RD3								
237	ENET_TXC_SOM_1V8	ENET_TXC	GPIO1_I023	SAI7_TX_DATA0	USDHC3_DATA1											
240	ENET2_RGMII_TXC_1V8	SAI1_TXD5	GPIO4_I017	SAI1_RX_DATA5 SAI6_RX_DATA0 SAI6_TX_DATA0				ENET1_R_GMII_TX_C								
241	ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	GPIO1_I022	SAI6_MC_LK	USDHC3_DATA0										SPDIF1_OUT	
242	ENET2_RGMII_TX_CTL_1V8	SAI1_TXD4	GPIO4_I016	SAI1_RX_DATA4 SAI6_RX_BCLK SAI6_TX_BCLK				ENET1_R_GMII_TX_CTL								
243	ENET_TD0_SOM_1V8	ENET_TD0	GPIO1_I021	SAI6_RX_BCLK	USDHC3_WP											
244	ENET2_RGMII_TD0_1V8	SAI1_TXD0	GPIO4_I012	SAI1_RX_DATA0				ENET1_R_GMII_TD0								
	ENET_TD1_SOM_1V8	ENET_TD1	GPIO1_I020	SAI6_RX_SYNC	USDHC3_CD_B											
246	ENET2_RGMII_TD1_1V8	SAI1_TXD1	GPIO1_I013	SAI1_RX_DATA1				ENET1_R_GMII_TD1								
247	ENET_TD2_SOM_1V8	ENET_TD2	GPIO1_I019	SAI6_RX_DATA0	USDHC3_DATA7											
248	ENET2_RGMII_TD2_1V8	SAI1_TXD2	GPIO4_I014	SAI1_RX_DATA2				ENET1_R_GMII_TD2								
249	ENET_TD3_SOM_1V8	ENET_TD3	GPIO1_I018	SAI6_TX_BCLK	USDHC3_DATA6											
250	ENET2_RGMII_TD3_1V8	SAI1_TXD3	GPIO4_I015	SAI1_RX_DATA3				ENET1_R_GMII_TD3								

5 SIGNAL DESCRIPTION PER BLOCK/INSTANCE

This chapter describes in detail the default SOM pins, the pin names, and the external interfaces per block-instance.

Pin Number:	Pin number on the VEST i.MX8M Plus SOM edge connector
Pin Name:	Pin name on the VEST i.MX8M Plus SOM edge connector
i.MX8M Plus Pad Name:	Pad name on i.MX8M Plus
Signal Type:	Type of Pin signal
Voltage Level:	Pin voltage level
Description:	Short pin description

5.1 CLOCK CONTROLLER MODULE (CCM)

The Clock Control Module (CCM) manages the on-chip module clocks. CCM receives clocks from PSSs and oscillators and creates clocks for the on-chip peripherals through a set of multiplexers, dividers, and gates. When entering or exiting a low power mode, the CCM automatically turns on and off PLLs and peripheral clocks.

The following table describes the external signals of CCM:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	Signal Type	Signal	Description
175	USB2_EN_1V8	GPIO1_IO14	1.8V	O	CCM_CLKO1	Observability clock 1 output
180	UART4_CTS_1V8	ECSPI2_MISO	1.8V	O		
130	CSI_MCLK_1V8	GPIO1_IO15	1.8V	O	CCM_CLKO2	Observability clock 2 output
178	UART4_RTS_1V8	ECSPI2_SSO	1.8V	O		
189	HP_DETECT_1V8	GPIO1_IO01	1.8V	O	CCM_REF_CLK_24M	24M oscillator clock output

Table 5-1: External Signals of CCM

5.2 ENHANCED CONFIGURABLE SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block.

The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). The ECSP's data FIFOs allows rapid data communication with fewer software interrupts.

The following table describes the external signals of ECSPI:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	ECSPI	Description
22	SD2_CLK	SD2_CLK	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_I004), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	ECSPI2_SCLK	SPI clock signal
24	SD2_CMD	SD2_CMD	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_I004), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	ECSPI2_MOSI	Master data out; slave data in
30	SD2_DATA2	SD2_DATA2	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_I004), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	ECSPI2_SSO	Chip select signal
32	SD2_DATA3	SD2_DATA3	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_I004), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	ECSPI2_MISO	Master data in; slave data out
46	ECSPI1_SSO_1V8	ECSPI1_SSO	1.8V	ECSPI1_SSO	Chip select signal
48	ECSPI1_MOSI_1V8	ECSPI1_MOSI	1.8V	ECSPI1_MOSI	Master data out; slave data in
50	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	ECSPI1_MISO	Master data in; slave data out
52	ECSPI1_SCLK_1V8	ECSPI1_SCLK	1.8V	ECSPI1_SCLK	SPI clock signal
174	UART4_RXD_1V8	ECSPI2_SCLK	1.8V	ECSPI2_SCLK	SPI clock signal
176	UART4_TXD_1V8	ECSPI2_MOSI	1.8V	ECSPI2_MOSI	Master data out; slave data in
178	UART4_RTS_1V8	ECSPI2_SSO	1.8V	ECSPI2_SSO	Chip select signal
180	UART4_CTS_1V8	ECSPI2_MISO	1.8V	ECSPI2_MISO	Master data in; slave data out
192	UART1_RXD_1V8	UART1_RXD	1.8V	ECSPI3_SCLK	SPI clock signal
194	UART1_TXD_1V8	UART1_TXD	1.8V	ECSPI3_MOSI	Master data out; slave data in
200	UART2_RXD_1V8	UART2_RXD	1.8V	ECSPI3_MISO	Master data in; slave data out
201	I2C4_SCL_1V8	I2C4_SCL	1.8V	ECSPI2_MISO	Master data in; slave data out
202	UART2_TXD_1V8	UART2_TXD	1.8V	ECSPI3_SSO	Chip select signal
203	I2C4_SDA_1V8	I2C4_SDA	1.8V	ECSPI2_SSO	Chip select signal
205	I2C2_SCL_1V8	I2C2_SCL	1.8V	ECSPI1_MISO	Master data in; slave data out
207	I2C2_SDA_1V8	I2C2_SDA	1.8V	ECSPI1_SSO	Chip select signal
209	I2C3_SCL_1V8	I2C3_SCL	1.8V	ECSPI2_SCLK	SPI clock signal
211	I2C3_SDA_1V8	I2C3_SDA	1.8V	ECSPI2_MOSI	Master data out; slave data in

Table 5-2: External Signals of ECSPI

5.3 ETHERNET MAC (ENET1)

The core implements a triple-speed 10/100/1000-Mbit/s Ethernet MAC compliant with the IEEE802.3-2002 standard. The MAC layer provides compatibility with half- or full-duplex 10/100-Mbit/s and full-duplex gigabit Ethernet LANs.

The MAC operation is fully programmable and can be used in a Network Interface Controller (NIC), bridging, or switching applications. The core implements the remote network monitoring (RMON) counters according to IETF RFC 2819.

The core also implements a hardware acceleration block to optimize the performance of network controllers providing TCP/IP, UDP, and ICMP protocol services. The acceleration block performs critical functions in hardware, without a large software overhead.

The core implements programmable embedded FIFOs that can provide buffering on the receive path for lossless flow control.

Advanced power management features are available with magic packet detection and programmable power-down modes.

A unified DMA (uDMA), internal to the ENET module, optimizes data transfer between the ENET core and the SoC, and supports an enhanced buffer descriptor programming model to support IEEE 1588 functionality.

The programmable Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications.

The following table describes the external signals of ENET1:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	ENET1	Description
1	NC or SD1_DATA3_1V8	SD1_DATA3	1.8V	ENET1_RGMII_RD1	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
3	NC or SD1_DATA2_1V8	SD1_DATA2	1.8V	ENET1_RGMII_RDO	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
5	NC or SD1_DATA1_1V8	SD1_DATA1	1.8V	ENET1_RGMII_TDO	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
7	NC or SD1_DATA0_1V8	SD1_DATA0	1.8V	ENET1_RGMII_TD1	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
8	NC or WLAN IRQ_1V8	SAI1_RXC	1.8V	ENET1_1588_EVENT_TO_OUT	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
9	NC or SD1_CMD_1V8	SD1_CMD	1.8V	ENET1_MDIO	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	ENET1	Description
10	NC or WLAN_EN_1V8	SAI1_RXDO	1.8V	ENET1_1588_EVEN_T1_IN	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
11	NC or SD1_CLK_1V8	SD1_CLK	1.8V	ENET1_MDC	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
21	NC or UART3_RTS_1V8	SD1_RESET_B	1.8V	ENET1_TX_CLK	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
23	NC or UART3_RXD_1V8	SD1_DATA7	1.8V	ENET1_RX_ER	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
27	NC or UART3_TXD_1V8	SD1_DATA6	1.8V	ENET1_RGMII_RX_CTL	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
42	GPIO4_IO03_1V8	SAI1_RXD1	1.8V	ENET1_1588_EVEN_T1_OUT	
92	GPIO4_IO00_1V8	SAI1_RXFS	1.8V	ENET1_1588_EVEN_TO_IN	
148	SAI2_MCLK_1V8	SAI2_MCLK	1.8V	ENET_QOS_1588_EVENT3_IN/ENET_QOS_1588_EVENT3_AUX_IN	
150	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	ENET_QOS_1588_EVENT3_OUT	
152	SAI2_TXD_1V8	SAI2_TXDO	1.8V	ENET_QOS_1588_EVENT2_IN/ENET_QOS_1588_EVENT2_AUX_IN	
154	SAI2_RXD_1V8	SAI2_RXDO	1.8V	ENET_QOS_1588_EVENT2_OUT	
170	GPIO4_IO20_1V8	SAI1_MCLK	1.8V	ENET1_TX_CLK	
215	ENET_nRST_1V8	SDA1_DATA4	1.8V	ENET1_RGMII_TX_CTL	
217	ENET_nINT_1V8	SD1_DATA5	1.8V	ENET1_TX_ER	SKUs without on board Ethernet PHY only
218	ENET2_RGMII_nINT_1V8	SAI1_TXD6	1.8V	ENET1_RX_ER	
220	ENET2_RGMII_MDIO_1V8	SAI1_RXD3	1.8V	ENET1_MDIO	
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2	1.8V	ENET1_MDC	
226	ENET2_RGMII_RXC_1V8	SAI1_TXC	1.8V	ENET1_RGMII_RXC	
228	ENET2_RGMII_RX_CTL_1V8	SAI1_TXFS	1.8V	ENET1_RGMII_RX_CTL	
230	ENET2_RGMII_RDO_1V8	SAI1_RXD4	1.8V	ENET1_RGMII_RDO	
232	ENET2_RGMII_RD1_1V8	SAI1_RXD5	1.8V	ENET1_RGMII_RD1	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	ENET1	Description
234	ENET2_RGMII_RD2_1V8	SAI1_RXD6	1.8V	ENET1_RGMII_RD2	
236	ENET2_RGMII_RD3_1V8	SAI1_RXD7	1.8V	ENET1_RGMII_RD3	
240	ENET2_RGMII_TXC_1V8	SAI1_TXD5	1.8V	ENET1_RGMII_TXC	
242	ENET2_RGMII_TX_CTL_1V8	SAI1_TXD4	1.8V	ENET1_RGMII_TX_CTL	
244	ENET2_RGMII_TD0_1V8	SAI1_TXD0	1.8V	ENET1_RGMII_TD0	
246	ENET2_RGMII_TD1_1V8	SAI1_TXD1	1.8V	ENET1_RGMII_TD1	
248	ENET2_RGMII_TD2_1V8	SAI1_TXD2	1.8V	ENET1_RGMII_TD2	
250	ENET2_RGMII_TD3_1V8	SAI1_TXD3	1.8V	ENET1_RGMII_TD3	

Table 5-3: External Signals of ENET1

5.4 FLEXIBLE CONTROLLER AREA NETWORK (FLEXCAN)

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

The CAN protocol was originally designed to be used as a vehicle serial data bus, meeting the specific real-time processing and reliable operation requirements in the EMI environment of a vehicle. The FlexCAN module is a full implementation of the CAN protocol specification. The CAN with the Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, that support both standard and extended message frames and long payloads.

The following table describes the external signals of FLEXCAN:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	FLEXCAN	Description
88	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	CAN1_TX	
90	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	CAN1_RX	
62	HDMI_HPD	HDMI_HPD	1.8V	CAN2_RX	
64	HDMI_CEC	HDMI_CEC	1.8V	CAN2_TX	
6	NC or BT_EN_1V8	SAI5_MCLK	1.8V	CAN2_RX	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
14	NC or SAI5_RXD_1V8	SAI5_RXD3	1.8V	CAN2_TX	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
94	GPIO4_IO22_1V8	SAI2_RXC	1.8V	CAN1_TX	
96	GPIO3_IO22_1V8	SAI5_RXD1	1.8V	CAN1_TX	
98	GPIO3_IO23_1V8	SAI5_RXD2	1.8V	CAN1_RX	
148	SAI2_MCLK_1V8	SAI2_MCLK	1.8V	CAN2_RX	
152	SAI2_RXD_1V8	SAI2_RXD0	1.8V	CAN2_TX	
156	SAI2_TXC_1V8	SAI2_TXC	1.8V	CAN1_RX	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	FLEXCAN	Description
182	CAN1_TX_1V8	SPDIF_TX	1.8V	CAN1_TX	
184	CAN1_RX_1V8	SPDIF_RX	1.8V	CAN1_RX	
186	CAN2_TX_1V8	UART3_RXD	1.8V	CAN2_TX	
188	CAN2_RX_1V8	UART3_TXD	1.8V	CAN2_RX	

Table 5-4: External Signals of FLEXCAN

5.5 GENERAL PURPOSE INPUT/OUTPUT (GPIO)

The general-purpose input/output (GPIO) provides dedicated general-purpose pins that can be user configured as either inputs or outputs.

When configured as an output, a write to an internal register controls the state driven on the output pin. When configured as an input, a read from an internal register detects the input state. Additionally, the GPIO peripheral can also produce CORE interrupts.

The following table describes the external signals of GPIO:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
1	NC or SD1_DATA3_1V8	SD1_DATA3	1.8V	GPIO2_IO5	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
3	NC or SD1_DATA2_1V8	SD1_DATA2	1.8V	GPIO2_IO4	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
4	NC or PWM_4_1V8	SAI5_RXFS	1.8V	GPIO3_IO19	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
5	NC or SD1_DATA1_1V8	SD1_DATA1	1.8V	GPIO2_IO3	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
6	NC or BT_EN_1V8	SAI5_MCLK	1.8V	GPIO3_IO25	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
7	NC or SD1_DATA0_1V8	SD1_DATA0	1.8V	GPIO2_IO2	For SKUs with an on-board WiFi/BT module, this pin is a NC.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
					NC. This pin is only available for SKUs without an on-board WiFi/BT module.
8	NC or WLAN IRQ_1V8	SAI1_RXC	1.8V	GPIO4_IO1	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
9	NC or SD1_CMD_1V8	SD1_CMD	1.8V	GPIO2_IO1	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
10	NC or WLAN_EN_1V8	SAI1_RXD0	1.8V	GPIO4_IO2	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
11	NC or SD1_CLK_1V8	SD1_CLK	1.8V	GPIO2_IO0	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
12	NC or SAI5_RXD_1V8	SAI5_RXD0	1.8V	GPIO3_IO21	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
14	NC or SAI5_TXD_1V8	SAI5_RXD3	1.8V	GPIO3_IO24	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
16	NC or SAI5_RXFS_1V8	SAI3_RXFS	1.8V	GPIO4_IO28	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
18	NC or SAI5_RXC_1V8	SAI3_RXC	1.8V	GPIO4_IO29	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
21	NC or UART3_RTS_1V8	SD1_RESET_B	1.8V	GPIO2_IO10	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
22	SD2_CLK	SD2_CLK	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V (SD_VSEL_1V8=Low) 1.8V (SD_VSEL_1V8=High)	GPIO2_IO13	
23	NC or UART3_RXD_1V8	SD1_DATA7	1.8V	GPIO2_IO9	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
24	SD2_CMD	SD2_CMD	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO14	
25	NC or UART3_CTS_1V8	SD1_STROBE	1.8V	GPIO2_IO11	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
26	SD2_DATA0	SD2_DATA0	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO15	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
27	NC or UART3_TXD_1V8	SD1_DATA6	1.8V	GPIO2_IO8	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
28	SD2_DATA1	SD2_DATA1	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO16	
30	SD2_DATA2	SD2_DATA2	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO17	
32	SD2_DATA3	SD2_DATA3	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO18	
34	SD2_WP	SD2_WP	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V (SD_VSEL_1V8=Low) 1.8V (SD_VSEL_1V8=High)	GPIO2_IO20	
36	SD2_nCD	SD2_CD_B	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO12	
38	SD2_RESET_B	SD2_RESET_B	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	GPIO2_IO19	
42	GPIO4_IO03_1V8	SAI1_RXD1	1.8V	GPIO4_IO3	
44	GPIO4_IO21_1V8	SAI2_RXFS	1.8V	GPIO4_IO21	
46	ECSPI1_SSO_1V8	ECSPI1_SSO	1.8V	GPIO5_IO9	
48	ECSPI1_MOSI_1V8	ECSPI1_MO_SI	1.8V	GPIO5_IO7	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
50	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	GPIO5_IO8	
52	ECSPI1_SCLK_1V8	ECSPI1_SCLK	1.8V	GPIO5_IO6	
62	HDMI_HPD	HDMI_HPD	1.8V	GPIO3_IO29	
64	HDMI_CEC	HDMI_CEC	1.8V	GPIO3_IO28	
88	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	GPIO3_IO26	
90	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	GPIO3_IO27	
92	GPIO4_IO00_1V8	SAI1_RXFS	1.8V	GPIO4_IO0	
94	GPIO4_IO22_1V8	SAI2_RXC	1.8V	GPIO4_IO22	
96	GPIO3_IO22_1V8	SAI5_RXD1	1.8V	GPIO3_IO22	
98	GPIO3_IO23_1V8	SAI5_RXD2	1.8V	GPIO3_IO23	
100	GPIO1_IO05_1V8	GPIO1_IO05	1.8V	GPIO1_IO5	
130	CSI_MCLK_1V8	GPIO1_IO15	1.8V	GPIO1_IO15	
132	USB1_EN_1V8	GPIO1_IO12	1.8V	GPIO1_IO12	
134	USB1_OC_1V8	GPIO1_IO13	1.8V	GPIO1_IO13	
138	USB1_ID_1V8	GPIO1_IO10	1.8V	GPIO1_IO10	
148	SAI2_MCLK_1V8	SAI2_MCLK	0V	GPIO4_IO27	GND
150	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	GPIO4_IO24	
152	SAI2_TXD_1V8	SAI2_TXD0	1.8V	GPIO4_IO26	
154	SAI2_RXD_1V8	SAI2_RXD0	1.8V	GPIO4_IO23	
156	SAI2_TXC_1V8	SAI2_TXC	1.8V	GPIO4_IO25	
170	GPIO4_IO20_1V8	SAI1_MCLK	1.8V	GPIO4_IO20	
174	UART4_RXD_1V8	ECSPI2_SCLK	1.8V	GPIO5_IO10	
175	USB2_EN_1V8	GPIO1_IO14	1.8V	GPIO1_IO14	
176	UART4_TXD_1V8	ECSPI2_MOSI	1.8V	GPIO5_IO11	
178	UART4_RTS_1V8	ECSPI2_SSO	1.8V	GPIO5_IO13	
179	USB2_ID_1V8	GPIO1_IO11	1.8V	GPIO1_IO11	
180	UART4_CTS_1V8	ECSPI2_MISO	1.8V	GPIO5_IO12	
182	CAN1_TX_1V8	SPDIF_TX	1.8V	GPIO5_IO3	
184	CAN1_RX_1V8	SPDIF_RX	1.8V	GPIO5_IO4	
186	CAN2_TX_1V8	UART3_RXD	1.8V	GPIO5_IO26	
188	CAN2_RX_1V8	UART3_RXD	1.8V	GPIO5_IO27	
189	HP_DETECT_1V8	GPIO1_IO01	1.8V	GPIO1_IO1	
192	UART1_RXD_1V8	UART1_RXD	1.8V	GPIO5_IO22	
193	PWM_3_1V8	SAI5_RXC	1.8V	GPIO3_IO20	
194	UART1_TXD_1V8	UART1_TXD	1.8V	GPIO5_IO23	
195	PWM_1_1V8	SPDIF_EXT_CLK	1.8V	GPIO5_IO5	
196	UART2_RTS_1V8	UART4_RXD	1.8V	GPIO5_IO29	
197	PWM_2_1V8	GPIO1_IO09	1.8V	GPIO1_IO9	
198	UART2_CTS_1V8	UART4_RXD	1.8V	GPIO5_IO28	
200	UART2_RXD_1V8	UART2_RXD	1.8V	GPIO5_IO24	
201	I2C4_SCL_1V8	I2C4_SCL	1.8V	GPIO5_IO20	
202	UART2_TXD_1V8	UART2_RXD	1.8V	GPIO5_IO25	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
203	I2C4_SDA_1V8	I2C4_SDA	1.8V	GPIO5_IO21	
205	I2C2_SCL_1V8	I2C2_SCL	1.8V	GPIO5_IO16	
206	SAI3_TXC_SOM_1V8	SAI3_TXC		GPIO5_IO0	For SKUs without Audio Codec only
207	I2C2_SDA_1V8	I2C2_SDA	1.8V	GPIO5_IO17	
208	SAI3_TXFS_SOM_1V8	SAI3_TXFS		GPIO4_IO31	For SKUs without Audio Codec only
209	I2C3_SCL_1V8	I2C3_SCL	1.8V	GPIO5_IO18	
210	SAI3_RXD_SOM_1V8	SAI3_RXD		GPIO4_IO30	For SKUs without Audio Codec only
211	I2C3_SDA_1V8	I2C3_SDA	1.8V	GPIO5_IO19	
212	SAI3_TXD_SOM_1V8	SAI3_TXD		GPIO5_IO1	For SKUs without Audio Codec only
214	SAI3_MCLK_SOM_1V8	SAI3_MCLK	1.8V	GPIO5_IO2	For SKUs without Audio Codec only
215	ENET_nRST_1V8	SDA1_DATA4	1.8V	GPIO2_IO6	
217	ENET_nINT_1V8	SD1_DATA5	1.8V	GPIO2_IO7	For SKUs without an on-board Ethernet PHY only
218	ENET2_RGMII_nINT_1V8	SAI1_RXD6	1.8V	GPIO4_IO18	
219	ENET_MIDO_1V8	ENET_MIDO	1.8V	GPIO1_IO17	For SKUs without an on-board Ethernet PHY only
220	ENET2_RGMII_MDI_O_1V8	SAI1_RXD3	1.8V	GPIO4_IO5	
221	ENET_MDC_1V8	ENET_MDC	1.8V	GPIO1_IO16	For SKUs without an on-board Ethernet PHY only
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2	1.8V	GPIO4_IO4	
223	NC or ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	1.8V	GPIO1_IO24	For SKUs without an on-board Ethernet PHY only
225	NC or ENET_RXC_SOM_1V8	ENET_RXC	1.8V	GPIO1_IO25	For SKUs without an on-board Ethernet PHY only
226	ENET2_RGMII_RXC_1V8	SAI1_TXC	1.8V	GPIO4_IO11	
228	ENET2_RGMII_RX_CTL_1V8	SAI1_TXFS	1.8V	GPIO4_IO10	
229	ENET_RDO_SOM_1V8	ENET_RDO	1.8V	GPIO1_IO26	For SKUs without an on-board Ethernet PHY only
230	ENET2_RGMII_RDO_1V8	SAI1_RXD4	1.8V	GPIO4_IO6	
231	ENET_RD1_SOM_1V8	ENET_RD1	1.8V	GPIO1_IO27	For SKUs without an on-board Ethernet PHY only
232	ENET2_RGMII_RD1_1V8	SAI1_RXD5	1.8V	GPIO4_IO7	
233	ENET_RD2_SOM_1V8	ENET_RD2	1.8V	GPIO1_IO28	For SKUs without an on-board Ethernet PHY only
234	ENET2_RGMII_RD2_1V8	SAI1_RXD6	1.8V	GPIO4_IO8	
235	ENET_RX3_SOM_1V8	ENET_RX3	1.8V	GPIO1_IO29	For SKUs without an on-board Ethernet PHY only

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	GPIO	Description
236	<i>ENET2_RGMII_RD3_1V8</i>	<i>SAI1_RXD7</i>	1.8V	<i>GPIO4_IO9</i>	
237	<i>ENET_TXC_SOM_1V8</i>	<i>ENET_TXC</i>	1.8V	<i>GPIO1_IO23</i>	For SKUs without an on-board Ethernet PHY only
240	<i>ENET2_RGMII_TXC_1V8</i>	<i>SAI1_TXD5</i>	1.8V	<i>GPIO4_IO17</i>	
241	<i>ENET_TX_CTL_SOM_1V8</i>	<i>ENET_TX_CTL</i>	1.8V	<i>GPIO1_IO22</i>	For SKUs without an on-board Ethernet PHY only
242	<i>ENET2_RGMII_TXC_TL_1V8</i>	<i>SAI1_TXD4</i>	1.8V	<i>GPIO4_IO16</i>	
243	<i>ENET_TDO_SOM_1V8</i>	<i>ENET_TXDO</i>	1.8V	<i>GPIO1_IO21</i>	For SKUs without an on-board Ethernet PHY only
244	<i>ENET2_RGMII_TDO_1V8</i>	<i>SAI1_TXDO</i>	1.8V	<i>GPIO4_IO12</i>	
245	<i>ENET_TD1_SOM_1V8</i>	<i>ENET_TD1</i>	1.8V	<i>GPIO1_IO20</i>	For SKUs without an on-board Ethernet PHY only
246	<i>ENET2_RGMII_TD1_1V8</i>	<i>SAI1_TXD1</i>	1.8V	<i>GPIO4_IO13</i>	
247	<i>ENET_TD2_SOM_1V8</i>	<i>ENET_TD2</i>	1.8V	<i>GPIO1_IO19</i>	For SKUs without an on-board Ethernet PHY only
248	<i>ENET2_RGMII_TD2_1V8</i>	<i>SAI1_TXD2</i>	1.8V	<i>GPIO4_IO14</i>	
249	<i>ENET_TD3_SOM_1V8</i>	<i>ENET_TD3</i>	1.8V	<i>GPIO1_IO18</i>	For SKUs without an on-board Ethernet PHY only
250	<i>ENET2_RGMII_TD3_1V8</i>	<i>SAI1_TXD3</i>	1.8V	<i>GPIO4_IO15</i>	

Table 5-5: External Signals of GPIO

5.6 HDMI

HDMI (c2.0a) can transfer uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25MHz up to 297MHz. HDMI can support several audio standards. It can support up to eight IEC60958 L-PCM audio channels, including IEC61937 compressed non-linear PCM and HBR (high bit rate) audio interfaces. HDMI has the capability of automatically setting the display's format configuration (intelligent link).

The following table describes the external signals of HDMI.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	HDMI	Description
74	<i>HDMI_TX1_P</i>	<i>HDMI_TX1_P</i>		<i>HDMI_TX1_P</i>	HDMI differential data 1 positive
62	<i>HDMI_HPD</i>	<i>HDMI_HPD</i>	1.8V	<i>HDMI_HPD/HDMI_HPD_O</i>	
64	<i>HDMI_CEC</i>	<i>HDMI_CEC</i>	1.8V	<i>HDMI_CEC</i>	
68	<i>HDMI_TX2_N</i>	<i>HDMI_TX2_N</i>		<i>HDMI_TX2_N</i>	HDMI differential data 2 negative
70	<i>HDMI_TX2_P</i>	<i>HDMI_TX2_P</i>		<i>HDMI_TX2_P</i>	HDMI differential data 2 positive
72	<i>HDMI_TX1_N</i>	<i>HDMI_TX1_N</i>		<i>HDMI_TX1_N</i>	HDMI differential data 1 negative
78	<i>HDMI_TX0_N</i>	<i>HDMI_TX0_N</i>		<i>HDMI_TX0_N</i>	HDMI differential data 0 negative

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	HDMI	Description
80	HDMI_TXO_P	HDMI_TXO_P		HDMI_TXO_P	HDMI differential data 0 positive
82	HDMI_TXC_N	HDMI_TXC_N		HDMI_TXC_N	HDMI clock differential negative
84	HDMI_TXC_P	HDMI_TXC_P		HDMI_TXC_P	HDMI clock differential positive
88	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	HDMI_SCL	
90	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	HDMI_SDA	

Table 5-6: External Signals of HDMI

5.7 I2C

The (I2C) provides functionality of a standard I2C slave and master. The I2C is designed to be compatible with the standard NXP I2C bus protocol.

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnections between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The following table describes the external signals of I2C:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	I2C	Description
198	UART2_CTS_1V8	UART4_RXD	1.8V	I2C6_SCL	
201	I2C4_SCL_1V8	I2C4_SCL	1.8V	I2C4_SCL	
88	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	I2C5_SCL	
90	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	I2C5_SDA	
62	HDMI_HPD	HDMI_HPD	1.8V	I2C6_SDA	
64	HDMI_CEC	HDMI_CEC	1.8V	I2C6_SCL	
1	NC or SD1_DATA3_1V8	SD1_DATA3	1.8V	I2C4_SDA	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
3	NC or SD1_DATA2_1V8	SD1_DATA2	1.8V	I2C4_SCL	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
4	NC or PWM_4_1V8	SA15_RXFS	1.8V	I2C6_SCL	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	I2C	Description
5	NC or SD1_DATA1_1V8	SD1_DATA1	1.8V	I2C6_SDA	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
6	NC or BT_EN_1V8	SAI5_MCLK	1.8V	I2C5_SDA	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
7	NC or SD1_DATA0_1V8	SD1_DATA0	1.8V	I2C6_SCL	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
9	NC or SD1_CMD_1V8	SD1_CMD	1.8V	I2C5_SDA	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
11	NC or SD1_CLK_1V8	SD1_CLK	1.8V	I2C5_SCL	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
12	NC or SAI5_RXD_1V8	SAI5_RXD0	1.8V	I2C5_SCL	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
21	NC or UART3_RTS_1V8	SD1_RESET_B	1.8V	I2C3_SCL	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	I2C	Description
23	NC or UART3_RXD_1V8	SD1_DATA7	1.8V	I2C2_SDA	<p>For variants with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for variants without an on-board WiFi/BT module.</p>
25	NC or UART3_CTS_1V8	SD1_STROBE	1.8V	I2C3_SDA	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
26	SD2_DATA0	SD2_DATA0	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V (SD_VSEL_1V8=Low) 1.8V (SD_VSEL_1V8=High)	I2C4_SDA	
27	NC or UART3_TXD_1V8	SD1_DATA6	1.8V	I2C2_SCL	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
28	SD2_DATA1	SD2_DATA1	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V (SD_VSEL_1V8=Low) 1.8V (SD_VSEL_1V8=High)	I2C4_SCL	
46	ECSPI1_SSO_1V8	ECSPI1_SSO	1.8V	I2C2_SDA	
50	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	I2C2_SCL	
174	UART4_RXD_1V8	ECSPI2_SCLK	1.8V	I2C3_SCL	
176	UART4_TXD_1V8	ECSPI2_MOSI	1.8V	I2C3_SDA	
178	UART4_RTS_1V8	ECSPI2_SSO	1.8V	I2C4_SDA	
180	UART4_CTS_1V8	ECSPI2_MISO	1.8V	I2C4_SCL	
182	CAN1_TX_1V8	SPDIF_TX	1.8V	I2C5_SCL	
184	CAN1_RX_1V8	SPDIF_RX	1.8V	I2C5_SDA	
185	I2C1_SCL_1V8	I2C1_SCL	1.8V	I2C1_SCL	I2C1 SCL
187	I2C1_SDA_1V8	I2C1_SDA	1.8V	I2C1_SDA	I2C1 SDA
193	PWM_3_1V8	SA15_RXC	1.8V	I2C6_SDA	
196	UART2_RTS_1V8	UART4_TXD	1.8V	I2C6_SDA	
198	UART2_CTS_1V8	UART4_RXD	1.8V	I2C6_SCL	
201	I2C4_SCL_1V8	I2C4_SCL	1.8V	I2C4_SCL	
203	I2C4_SDA_1V8	I2C4_SDA	1.8V	I2C4_SDA	
205	I2C2_SCL_1V8	I2C2_SCL	1.8V	I2C2_SCL	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	I2C	Description
207	I2C2_SDA_1V8	I2C2_SDA	1.8V	I2C2_SDA	
209	I2C3_SCL_1V8	I2C3_SCL	1.8V	I2C3_SCL	
211	I2C3_SDA_1V8	I2C3_SDA	1.8V	I2C3_SDA	

Table 5-7: External Signals of I2C

5.8 JOINT TEST ACTION GROUP(JTAG)

There is only one JTAG on the chip that is switched between two JTAG modes. The modes are selected via the JTAG_MOD pin.

- Debug mode: JTAG_MOD == 0, DAP is the only TAP controller in the daisy chain. SJC will be attached to JTAG-AP of DAP.
- Test mode: JTAG_MOD == 1, SJC is the only TAP controller in the daisy chain. 1149.1-compliant, and support 1149.6 AC coupled test.

When the JTAG interface is in Debug Mode, it can be operated in a standard 5-pin JTAG interface. CJTAG/SWD interface is not supported by this chip.

The following table describes the external signals of the JTAG:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	JTAG	Description
160	JTAG_TDI_1V8	JTAG_TDI	1.8V	JTAG_TDI	JTAG TDI
162	JTAG_TDO_1V8	JTAG_TDO	1.8V	JTAG_TDO	JTAG TDO
164	JTAG_TMS_1V8	JTAG_TMS	1.8V	JTAG_TMS	JTAG TMS
166	JTAG_TCK_1V8	JTAG_TCK	1.8V	JTAG_TCK	JTAG TCK
168	JTAG_MODE_1V8	JTAG_MODE	1.8V	JTAG_MODE	JTAG MODE

Table 5-8: External Signals of JTAG

5.9 LVDS DISPLAY BRIDGE (LDB)

This chip supports one LVDS Tx display and Pixel Mapper. The LVDS port may be used as follows:

- Single channel (4 lanes) supports resolutions up to 720p60.
- Dual asynchronous channels (8 data, 2 clocks)
 - Supports resolutions up to 1920x1200p60.
 - Intended for a single panel with two interfaces, when transferring across two channels (even pixel/odd pixel).
 - The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream.

The following table describes the external signals of LVDS:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	LVDS	Description
31	LVDS0_TX3_N	LVDS0_D3_N	LVDS0_D3_N	LVDS0 differential pair 3 negative
33	LVDS0_TX3_P	LVDS0_D3_P	LVDS0_D3_P	LVDS0 differential pair 3 positive

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	LVDS	Description
35	LVDS0_TX2_N	LVDS0_D2_N	LVDS0_D2_N	LVDS0 differential pair 2 negative
37	LVDS0_TX2_P	LVDS0_D2_P	LVDS0_D2_P	LVDS0 differential pair 2 positive
41	LVDS0_CLK_N	LVDS0_CLK_N	LVDS0_CLK_N	LVDS0 clock differential pair negative
43	LVDS0_CLK_P	LVDS0_CLK_P	LVDS0_CLK_P	LVDS0 clock differential pair positive
47	LVDS0_TX1_N	LVDS0_D1_N	LVDS0_D1_N	LVDS0 differential pair 1 negative
49	LVDS0_TX1_P	LVDS0_D1_P	LVDS0_D1_P	LVDS0 differential pair 1 positive
51	LVDS0_RX0_N	LVDS0_D0_N	LVDS0_D0_N	LVDS0 differential pair 0 negative
53	LVDS0_RX0_P	LVDS0_D0_P	LVDS0_D0_P	LVDS0 differential pair 0 positive
57	LVDS1_RX3_N	LVDS1_D3_N	LVDS1_D3_N	LVDS1 differential pair 3 negative
61	LVDS1_RX2_N	LVDS1_D2_N	LVDS1_D2_N	LVDS1 differential pair 2 negative
59	LVDS1_RX3_P	LVDS1_D3_P	LVDS1_D3_P	LVDS1 differential pair 3 positive
67	LVDS1_CLK_N	LVDS1_CLK_N	LVDS1_CLK_N	LVDS1 clock differential pair negative
69	LVDS1_CLK_P	LVDS1_CLK_P	LVDS1_CLK_P	LVDS1 clock differential pair positive
63	LVDS1_RX2_P	LVDS1_D2_P	LVDS1_D2_P	LVDS1 differential pair 2 positive
73	LVDS1_RX1_N	LVDS1_D1_N	LVDS1_D1_N	LVDS1 differential pair 1 negative
75	LVDS1_RX1_P	LVDS1_D1_P	LVDS1_D1_P	LVDS1 differential pair 1 positive
77	LVDS1_RX0_N	LVDS1_D0_N	LVDS1_D0_N	HDMI differential data 0 negative
79	LVDS1_RX0_P	LVDS1_D0_P	LVDS1_D0_P	LVDS1 differential pair 0 positive

Table 5-9: External Signals of LVDS

5.10 MIPI-CAMERA SERIAL INTERFACE HOST CONTROLLER (MIPI_CSI)

The MIPI Camera Serial Interface (MIPI_CSI2) works with MIPI DPHY module to connect to the host processor.

MIPI_CSI2 supports RAW, YUV and RGB image formats when used in conjunction with an output to ISI (Image Sensing Interface) or ISP (Image Signal Processing).

The chip supports two 4-lane MIPI CSI2 camera inputs. The key features of the MIPI CSI2 (controller and PHY) include:

- Compliant to MIPI-CSI2 standard
- Support up to 4 data lanes
- When one ISP is used, MIPI CSI interface 1 supports:
 - Pixel clock up to 400MHz at nominal voltage and 500MHz at overdrive voltage
 - 80Mbps - 1.5Gbps per lane data rate in high speed operation
- When two ISPs are used, both MIPI CSI interfaces support:
 - Pixel clock up to 266MHz at nominal and overdrive voltage
 - 80Mbps - 1.5Gbps per lane data rate in high speed operation (the maximum speed of 1.5Gbps per lane is only supported when only 2 data lanes are used)

- When used in conjunction with an ISP output, the RAW8, RAW10, RAW12, and RAW14 image formats are supported
- When used in conjunction with an ISI output, the YUV420 (8-bit and 10-bit), YUV422 (8-bit and 10-bit), RGB565, RGB666, RGB888 image formats are supported
- Support for a 10Mbps data rate in low power operation

The following table describes the external signals of MIPI_CSI:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	MIPI_CSI	Description
83	CSI2_D0_N	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N	MIPI CSI2 differential pair 0 negative
85	CSI2_D0_P	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P	MIPI CSI2 differential pair 0 positive
87	CSI2_D1_N	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N	MIPI CSI2 differential pair 1 negative
89	CSI2_D1_P	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P	MIPI CSI2 differential pair 1 positive
93	CSI2_CLK_N	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N	MIPI CSI2 clock differential pair negative
95	CSI2_CLK_P	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P	MIPI CSI2 clock differential pair positive
99	CSI2_D2_N	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N	MIPI CSI2 differential pair 2 negative
101	CSI2_D2_P	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P	MIPI CSI2 differential pair 2 positive
103	CSI2_D3_N	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N	MIPI CSI2 differential pair 3 negative
104	CSI1_D3_P	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P	MIPI CSI1 differential pair 3 positive
105	CSI2_D3_P	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P	MIPI CSI2 differential pair 3 positive
106	CSI1_D3_N	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N	MIPI CSI1 differential pair 3 negative
108	CSI1_D2_P	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P	MIPI CSI1 differential pair 2 positive
110	CSI1_D2_N	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N	MIPI CSI1 differential pair 2 negative
114	CSI1_CLK_P	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N	MIPI CSI1 clock differential pair negative
116	CSI1_CLK_N	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P	MIPI CSI1 clock differential pair positive
120	CSI1_D1_P	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P	MIPI CSI1 differential pair 1 positive
122	CSI1_D1_N	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N	MIPI CSI1 differential pair 1 negative
124	CSI1_D0_P	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P	MIPI CSI1 differential pair 0 negative

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	MIPI_CSI	Description
126	CSI1_DO_N	MIPI_CSI1_DO_N	MIPI_CSI1_DO_N	MIPI CSI1 differential pair 0 positive

Table 5-10: External Signals of MIPI_CSI

5.11 MIPI-DISPLAY SERIAL INTERFACE HOST CONTROLLER (MIPI_DSI)

MIPI Display Serial Interface (DSI) is a flexible, high-performance core that allows communication with MIPI DSI compliant peripherals.

This chip supports one 4-lane MIPI DSI display with pixels from the LCDIF. The key features of the MIPI DSI (controller and PHY) include:

- Compliant to MIPI-DSI standard v1.2
- Supports up to 4 data lanes
- Maximum resolution limited to resolutions achievable with a 250MHz pixel clock and active pixel rate of 200Mpixel/s with 24-bit RGB. This includes resolutions show below:
 - 1080 p60
 - WUXGA (1920x1200) at 60 Hz
 - 1920x1440 at 60 Hz
 - UWHD (2560x1080) at 60 Hz
 - WQHD (2560x1440) can be supported in a reduced blanking mode
- Supports 80Mbps - 1.5Gbps data rate in high speed operation
- Supports 10Mbps data rate in low power operation

The following table describes the external signals of MIPI_DSI:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	MIPI_DSI	Description
109	DSI_D3_N	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N	MIPI DSI differential pair 3 negative
111	DSI_D3_P	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P	MIPI DSI differential pair 3 positive
113	DSI_D2_N	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N	MIPI DSI differential pair 2 negative
115	DSI_D2_P	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P	MIPI DSI differential pair 2 positive
119	DSI_CLK_N	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N	MIPI DSI clock differential negative
121	DSI_CLK_P	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P	MIPI DSI clock differential positive
125	DSI_D1_N	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N	MIPI DSI differential pair 1 negative
127	DSI_D1_P	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P	MIPI DSI differential pair 1 positive

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	MIPI_DSI	Description
129	DSI_D0_N	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N	MIPI DSI differential pair 0 negative
131	DSI_D0_P	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P	MIPI DSI differential pair 0 positive

Table 5-11: External Signals of MIPI_DSI

5.12 PCI EXPRESS (PCIE)

The PCIe PHY IP core is used for PCI-Express (PCIe) applications. The transceiver in the core performs the following functions:

- Serializes the 8b/10b encoded data for transmission for Gen1 and Gen2 operation, and 128b/130b encoded data for Gen3
- De-serializes the received code groups

When transmitting the data, the transceiver performs these functions:

- Accepts four 10-bit 8b/10b encoded transmit characters or four 8-bit 128b/130b encoded data
- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 8.0 Gb/s

When receiving the data, the transceiver performs these functions:

- Samples the received serial data on the RXP/RXN differential inputs
- Deserializes it into four 10-bit(or 8b-bit) received characters

PCIe PHY core has on-chip PLL circuitry for synthesis of the baud-rate transmitter clocks, and extraction of the retimed clocks from the received serial stream.

The following table describes the external signals of PCIe:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	PCIE	Description
135	PCIE_TX_N	PCIE_TXN_N	PCIE1_TXN_N	PCIe differential transmit negative
137	PCIE_TX_P	PCIE_TXN_P	PCIE1_TXN_P	PCIe differential transmit positive
139	PCIE_RX_N	PCIE_RXN_N	PCIE1_RXN_N	PCIe differential receive negative
141	PCIE_RX_P	PCIE_RXN_P	PCIE1_RXN_P	PCIe differential receive positive
145	PCIE_CLK_N	PCIE_REF_PAD_CLK_N	PCIE1_REF_PAD_CLK_N	PCIe clock differential negative
147	PCIE_CLK_P	PCIE_REF_PAD_CLK_P	PCIE1_REF_PAD_CLK_P	PCIe clock differential positive
198	UART2_CTS_1V8	UART4_RXD	PCIE1_CLKREQ_B	
201	I2C4_SCL_1V8	I2C4_SCL	PCIE1_CLKREQ_B	

Table 5-12: External Signals of PCIe

5.13 PDM MICROPHONE INTERFACE (PDM)

The Pulse Density Modulated Microphone Interface is common way to deliver audio from microphones to a processor in, several applications such as mobile telephones. However, current digital-audio systems use multibit audio signal (also known as multibit PCM) to represent the signal. This block implements the required digital interface to provide a 24-bits audio signal from a PDM microphone bitstream in a configurable output sampling rate.

The implementation of this digital interface is based on the application of hardware digital signal processing techniques. The PDM Microphone Interface architecture was designed to save gate count and minimize power consumption. It implements a series of filters to transform a PDM bitstream to a 24-bit PCM audio signal.

The whole module is designed to work in multichannel mode. All channels have the same configuration, but each input channel can be turned on/off independently.

The following table describes the external signals of PDM:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PDM	Description
8	NC or WLAN IRQ_1V8	SAI1_RXC	1.8V	PDM_CLK	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
10	NC or WLAN EN_1V8	SAI1_RXDO	1.8V	PDM_BIT_STREAM0	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
12	NC or SAI5_RXD_1V8	SAI5_RXDO	1.8V	PDM_BIT_STREAM0	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
14	NC or SAI5_TXD_1V8	SAI5_RXD3	1.8V	PDM_BIT_STREAM3	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
16	NC or SAI5_RXFS_1V8	SAI3_RXFS	1.8V	PDM_BIT_STREAM0	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
18	NC or SAI5_RXC_1V8	SAI3_RXC	1.8V	PDM_CLK	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs Without an on-board WiFi/BT module.</p>
24	SD2_CMD	SD2_CMD	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8 =Low) 1.8V(SD_VSEL_1V8 =High)	PDM_CLK	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PDM	Description
26	SD2_DATA0	SD2_DATA0	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8 =Low) 1.8V(SD_VSEL_1V8 =High)	PDM_BIT_STREAM0	
28	SD2_DATA1	SD2_DATA1	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8 =Low) 1.8V(SD_VSEL_1V8 =High)	PDM_BIT_STREAM1	
30	SD2_DATA2	SD2_DATA2	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8 =Low) 1.8V(SD_VSEL_1V8 =High)	PDM_BIT_STREAM2	
32	SD2_DATA3	SD2_DATA3	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8 =Low) 1.8V(SD_VSEL_1V8 =High)	PDM_BIT_STREAM3	
42	GPIO4_IO03_1V8	SAI1_RXD1	1.8V	PDM_BIT_STREAM1	
44	GPIO4_IO21_1V8	SAI2_RXFS	1.8V	PDM_BIT_STREAM2	
94	GPIO4_IO22_1V8	SAI2_RXC	1.8V	PDM_BIT_STREAM1	
96	GPIO3_IO22_1V8	SAI5_RXD1	1.8V	PDM_BIT_STREAM1	
98	GPIO3_IO23_1V8	SAI5_RXD2	1.8V	PDM_BIT_STREAM2	
150	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	PDM_BIT_STREAM2	
154	SAI2_RXD_1V8	SAI2_RXD0	1.8V	PDM_BIT_STREAM3	
156	SAI2_TXC_1V8	SAI2_TXC	1.8V	PDM_BIT_STREAM1	
193	PWM_3_1V8	SAI5_RXC	1.8V	PDM_CLK	
206	SAI3_TXC_SOM_1V8	SAI3_TXC		PDM_BIT_STREAM2	For SKUs without an Audio Codec
208	SAI3_TXFS_SOM_1V8	SAI3_TXFS		PDM_BIT_STREAM3	For SKUs without an Audio Codec
210	SAI3_RXD_SOM_1V8	SAI3_RXD		PDM_BIT_STREAM1	For SKUs without an Audio Codec
219	ENET_MIDO_1V8	ENET_MIDO	1.8V	PDM_BIT_STREAM3	For SKUs without an on-board Ethernet PHY
220	ENET2_RGMII_MDIO_1V8	SAI1_RXD3	1.8V	PDM_BIT_STREAM3	
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2	1.8V	PDM_BIT_STREAM2	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PDM	Description
223	NC or ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	1.8V	PDM_BIT_STREAM3	For SKUs without an on-board Ethernet PHY
225	NC or ENET_RXC_SOM_1V8	ENET_RXC	1.8V	PDM_BIT_STREAM2	For SKUs without an on-board Ethernet PHY
229	ENET_RDO_SOM_1V8	ENET_RDO	1.8V	PDM_BIT_STREAM1	For SKUs without an on-board Ethernet PHY
231	ENET_RD1_SOM_1V8	ENET_RD1	1.8V	PDM_BIT_STREAM0	For SKUs without an on-board Ethernet PHY
233	ENET_RD2_SOM_1V8	ENET_RD2	1.8V	PDM_CLK	For SKUs without an on-board Ethernet PHY
243	ENET_TD0_SOM_1V8	ENET_TXDO	1.8V	PDM_CLK	For SKUs without an on-board Ethernet PHY
245	ENET_TD1_SOM_1V8	ENET_TD1	1.8V	PDM_BIT_STREAM0	For SKUs without an on-board Ethernet PHY
247	ENET_TD2_SOM_1V8	ENET_TD2	1.8V	PDM_BIT_STREAM1	For SKUs without an on-board Ethernet PHY
249	ENET_TD3_SOM_1V8	ENET_TD3	1.8V	PDM_BIT_STREAM2	For SKUs without an on-board Ethernet PHY

Table 5-13: External Signals of PDM

5.14 PULSE WIDTH MODULATION (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and it is optimized to generate sound from stored sampled audio images. It uses 16-bit resolution and a 4 x 16 data FIFO.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configurable output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

The following table describes the external signals of PWM:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PWM	Description
4	NC or PWM_4_1V8	SAI5_RXFS	1.8V	PWM4_OUT	<p>For SKUs with an on-board WiFi/BT module, this pin is NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>

6	NC or BT_EN_1V8	SAI5_MCLK	1.8V	PWM1_OUT	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
12	NC or SAI5_RXD_1V8	SAI5_RXDO	1.8V	PWM2_OUT	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
130	CSI_MCLK_1V8	GPIO1_IO15	1.8V	PWM4_OUT	
134	USB1_OC_1V8	GPIO1_IO13	1.8V	PWM2_OUT	
138	USB1_ID_1V8	GPIO1_IO10	1.8V	PWM3_OUT	
175	USB2_EN_1V8	GPIO1_IO14	1.8V	PWM3_OUT	
179	USB2_ID_1V8	GPIO1_IO11	1.8V	PWM2_OUT	
182	CAN1_TX_1V8	SPDIF_TX	1.8V	PWM3_OUT	
184	CAN1_RX_1V8	SPDIF_TX	1.8V	PWM2_OUT	
189	HP_DETECT_1V8	GPIO1_IO01	1.8V	PWM1_OUT	
193	PWM_3_1V8	SAI5_RXC	1.8V	PWM3_OUT	
195	PWM_1_1V8	SPDIF_EXT_CLK	1.8V	PWM1_OUT	
197	PWM_2_1V8	GPIO1_IO09	1.8V	PWM2_OUT	
201	I2C4_SCL_1V8	I2C4_SCL	1.8V	PWM2_OUT	
203	I2C4_SDA_1V8	I2C4_SDA	1.8V	PWM1_OUT	
209	I2C3_SCL_1V8	I2C3_SCL	1.8V	PWM4_OUT	
211	I2C3_SDA_1V8	I2C3_SDA	1.8V	PWM3_OUT	
214	SAI3_MCLK_SOM_1V8	SAI3_MCLK	1.8V	PWM4_OUT	For SKUs without an Audio Codec only

Table 5-14: External Signals of PWM

5.15 SYNCHRONOUS AUDIO INTERFACE (SAI)

The Synchronous Audio Interface (SAI) provides full-duplex serial interfaces with frame synchronization formats such as I2S, AC97, TDM, and codec/DSP interfaces.

The following table describes the external signals of SAI:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SAI	Description
4	NC or PWM_4_1V8	SAI5_RXFS	1.8V	SAI5_RX_SYNC/SAI1_TX_DAT_A0	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SAI	Description
6	NC or BT_EN_1V8	SAI5_MCLK	1.8V	SAI5_MCLK/SAI1_TX_BCLK	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
8	NC or WLAN IRQ_1V8	SAI1_RXC	1.8V	SAI1_RX_BCLK	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
10	NC or WLAN_EN_1V8	SAI1_RXDO	1.8V	SAI1_RX_DATA0/SAI1_TX_DATA1	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
12	NC or SAI5_RXD_1V8	SAI5_RXDO	1.8V	SAI5_RX_DATA/SAI1_TX_DATA2	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
14	NC or SAI5_TXD_1V8	SAI5_RXD3	1.8V	SAI5_RX_DATA3/SAI1_TX_DATA5/SAI1_TX_SYNC/SAI5_TX_DATA0	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
16	NC or SAI5_RXFS_1V8	SAI3_RXFS	1.8V	SAI3_RX_SYNC/SAI2_RX_DATA1/SAI5_RX_SYNC/SAI3_RX_DATA1	For SKUs with an on-board WiFi/BT module, this pin is NC. This pin is only available for SKUs without an on-board WiFi/BT module.
18	NC or SAI5_RXC_1V8	SAI3_RXC	1.8V	SAI3_RX_BCLK/SAI2_RX_DATA2/SAI5_RX_BCLK	For Variants with an on-board WiFi/BT module, this pin is a NC. This pin is only available for variants without an on-board WiFi/BT module.
42	GPIO4_IO03_1V8	SAI1_RXD1	1.8V	SAI1_RX_DATA1	
44	GPIO4_IO21_1V8	SAI2_RXFS	1.8V	SAI2_RX_SYNC/SAI5_TX_SYNC/SAI5_TX_DATA1/SAI2_RX_DATA1	
46	ECSPI1_SS0_1V8	ECSPI1_SS0	1.8V	SAI7_TX_SYNC	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SAI	Description
48	ECSPI1_MOSI_1V8	ECSPI1_M_OSI	1.8V	SAI7_RX_BCLK	
50	ECSPI1_MISO_1V8	ECSPI1_MI_SO	1.8V	SAI7_RX_DATA0	
52	ECSPI1_SCLK_1V8	ECSPI1_SC_LK	1.8V	SAI7_RX_SYNC	
92	GPIO4_IO00_1V8	SAI1_RXFS	1.8V	SAI1_RX_SYNC	
94	GPIO4_IO22_1V8	SAI2_RXC	1.8V	SAI2_RX_BCLK/SAI5_TX_BCLK	
96	GPIO3_IO22_1V8	SAI5_RXD1	1.8V	SAI5_RX_DATA1/SAI1_TX_DADA3/SAI1_TX_SYNC/SAI5_TX_SYNC	
98	GPIO3_IO23_1V8	SAI5_RXD2	1.8V	SAI5_RX_DATA2/SAI1_TX_DADA4/SAI1_TX_SYNC/SAI5_TX_BCLK	
148	SAI2_MCLK_1V8	SAI2_MCLK	0V	SAI2_MCLK/SAI5_MCLK/SAI3_MCLK	GND
150	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	SAI2_TX_SYNC/SAI5_TX_DATA1/SAI2_TX_DATA1	
152	SAI2_TXD_1V8	SAI2_TXD0	1.8V	SAI2_TX_DATA0/SAI5_TX_DATA3	
154	SAI2_RXD_1V8	SAI2_RXD0	1.8V	SAI2_RX_DATA0/SAI5_TX_DATA0/SAI2_TX_DATA1	
156	SAI2_TXC_1V8	SAI2_TXC	1.8V	SAI2_TX_BCLK/SAI5_TX_DATA2	
170	GPIO4_IO20_1V8	SAI1_MCLK	1.8V	SAI1_MCLK/SAI1_TX_BCLK	
174	UART4_RXD_1V8	ECSPI2_SC_LK	1.8V	SAI7_TX_BCLK	
176	UART4_TXD_1V8	ECSPI2_M_OSI	1.8V	SAI7_TX_DATA0	
180	UART4_CTS_1V8	ECSPI2_MI_SO	1.8V	SAI7_MCLK	
193	PWM_3_1V8	SAI5_RXC	1.8V	SAI5_RX_BCLK/SAI1_TX_DATA1	
206	SAI3_TXC_SOM_1V8	SAI3_TXC		SAI3_TX_BCLK/SAI2_TX_DATA2/SAI5_RX_DATA2	For SKUs without an Audio Codec only
208	SAI3_TXFS_SOM_1V8	SAI3_TXFS		SAI3_TX_SYNC/SAI2_TX_DATA1/SAI5_RX_DATA1/SAI3_TX_DATA1	For SKUs without an Audio Codec only
210	SAI3_RXD_SOM_1V8	SAI3_RXD		SAI3_RX_DATA0/SAI2_RX_DADA3/SAI5_RX_DATA0	For SKUs without an Audio Codec only
212	SAI3_TXD_SOM_1V8	SAI3_TXD		SAI3_TX_DATA0/SAI2_TX_DADA3/SAI5_RX_DATA3	For SKUs without an Audio Codec only
214	SAI3_MCLK_SOM_1V8	SAI3_MCLK	1.8V	SAI3_MCLK/SAI5_MCLK	For SKUs without an Audio Codec only
218	ENET2_RGMII_nINT_1V8	SAI1_RXD6	1.8V	SAI1_TX_DATA6/SAI6_RX_SYNC/SAI6_TX_SYNC	
219	ENET_MIDO_1V8	ENET_MID_O	1.8V	SAI6_TX_SYNC	For SKUs without an on-board Ethernet PHY only
220	ENET2_RGMII_MDI_O_1V8	SAI1_RXD3	1.8V	SAI1_RX_DATA3	
221	ENET_MDC_1V8	ENET_MDC	1.8V	SAI6_TX_DATA0	For SKUs without an on-board Ethernet PHY only
222	ENET2_RGMII_MDC_1V8	SAI1_RXD2	1.8V	SAI1_RX_DATA2	
223	NC or ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	1.8V	SAI7_TX_SYNC	For SKUs without an on-board Ethernet PHY only

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SAI	Description
225	<i>NC or ENET_RXC_SOM_1V8</i>	ENET_RXC	1.8V	SAI7_TX_BCLK	For SKUs without an on-board Ethernet PHY only
226	<i>ENET2_RGMII_RXC_1V8</i>	SAI1_TXC	1.8V	SAI1_TX_BCLK	
228	<i>ENET2_RGMII_RX_CTL_1V8</i>	SAI1_TXFS	1.8V	SAI1_TX_SYNC	
229	<i>ENET_RDO_SOM_1V8</i>	ENET_RDO	1.8V	SAI7_RX_DATA0	For SKUs without an on-board Ethernet PHY only
230	<i>ENET2_RGMII_RDO_1V8</i>	SAI1_RXD4	1.8V	<i>SAI1_RX_DATA4/SAI6_RX_BCLK/SAI6_RX_BCLK</i>	
231	<i>ENET_RD1_SOM_1V8</i>	ENET_RD1	1.8V	SAI7_RX_SYNC	For SKUs without an on-board Ethernet PHY only
232	<i>ENET2_RGMII_RD1_1V8</i>	SAI1_RXD5	1.8V	<i>SAI1_RX_DATA5/SAI6_RX_DATA0/SAI1_RX_SYNC</i>	
233	<i>ENET_RD2_SOM_1V8</i>	ENET_RD2	1.8V	SAI7_RX_BCLK	For SKUs without an on-board Ethernet PHY only
234	<i>ENET2_RGMII_RD2_1V8</i>	SAI1_RXD6	1.8V	<i>SAI1_RX_DATA6/SAI6_RX_SYNC/SAI6_RX_SYNC</i>	
235	<i>ENET_RX3_SOM_1V8</i>	ENET_RX3	1.8V	SAI7_MCLK	For SKUs without an on-board Ethernet PHY only
236	<i>ENET2_RGMII_RD3_1V8</i>	SAI1_RXD7	1.8V	<i>SAI1_RX_DATA7/SAI6_MCLK/SAI1_TX_SYNC/SAI1_TX_DATA4</i>	
237	<i>ENET_TXC_SOM_1V8</i>	ENET_TXC	1.8V	SAI7_TX_DATA0	For SKUs without an on-board Ethernet PHY only
240	<i>ENET2_RGMII_TXC_1V8</i>	SAI1_TXD5	1.8V	<i>SAI1_TX_DATA5/SAI6_RX_DATA0/SAI6_TX_DATA0</i>	
241	<i>ENET_TX_CTL_SOM_1V8</i>	ENET_TX_CTL	1.8V	SAI6_MCLK	For SKUs without on board Ethernet PHY only
242	<i>ENET2_RGMII_TXC_CTL_1V8</i>	SAI1_TXD4	1.8V	<i>SAI1_TX_DATA4/SAI6_RX_BCLK/SAI6_TX_BCLK</i>	
243	<i>ENET_TD0_SOM_1V8</i>	ENET_TXD0	1.8V	SAI6_RX_BCLK	For SKUs without an on-board Ethernet PHY only
244	<i>ENET2_RGMII_TD0_1V8</i>	SAI1_TXD0	1.8V	SAI1_TX_DATA0	
245	<i>ENET_TD1_SOM_1V8</i>	ENET_TD1	1.8V	SAI6_RX_SYNC	For SKUs without an on-board Ethernet PHY only
246	<i>ENET2_RGMII_TD1_1V8</i>	SAI1_TXD1	1.8V	SAI1_TX_DATA1	
247	<i>ENET_TD2_SOM_1V8</i>	ENET_TD2	1.8V	SAI6_RX_DATA0	For SKUs without an on-board Ethernet PHY only
248	<i>ENET2_RGMII_TD2_1V8</i>	SAI1_TXD2	1.8V	SAI1_TX_DATA2	
249	<i>ENET_TD3_SOM_1V8</i>	ENET_TD3	1.8V	SAI6_TX_BCLK	For SKUs without an on-board Ethernet PHY only
250	<i>ENET2_RGMII_TD3_1V8</i>	SAI1_TXD3	1.8V	SAI1_TX_DATA3	

Table 5-15: External Signals of SAI

5.16 SONY PHILLIPS DIGITAL INTERFACE (SPDIF)

SPDIF supports raw capture mode that can save all incoming bits into an audio buffer.

SPDIF Receiver: Support for 32kHz - 192kHz sample rate

SPDIF Transmitter: Support for 32kHz - 192kHz data transmit rate.

The following table describes the external signals of SPDIF:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SPDIF	Description
16	NC or SAI5_RXFS_1V8	SAI3_RXFS	1.8V	SPDIF1_IN	For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.
30	SD2_DATA2	SD2_DATA2	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	SPDIF1_OUT	
32	SD2_DATA3	SD2_DATA3	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	SPDIF1_IN	
182	CAN1_TX_1V8	SPDIF_TX	1.8V	SPDIF1_OUT	
184	CAN1_RX_1V8	SPDIF_RX	1.8V	SPDIF1_IN	
195	PWM_1_1V8	SPDIF_EXT_CLK	1.8V	SPDIF1_EXT_CLK	
212	SAI3_TXD_SOM_1V8	SAI3_TXD		SPDIF1_EXT_CLK	For SKUs without an Audio Codec only
214	SAI3_MCLK_SOM_1V8	SAI3_MCLK	1.8V	SPDIF1_OUT SPDIF1_IN	For SKUs without an Audio Codec only
235	ENET_RX3_SOM_1V8	ENET_RX3	1.8V	SPDIF1_IN	For SKUs without an on-board Ethernet PHY only
241	ENET_TX_CTL_SOM_1V8	ENET_TX_CTL	1.8V	SPDIF1_OUT	For SKUs without an on-board Ethernet PHY only

Table 5-16: External Signals of SPDIF

5.17 UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

The Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter and an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.

The UART supports NRZ encoding format, RS485 compatible 9-bit data format and IrDA-compatible infrared slow data rate (SIR) format.

The following table describes the external signals of UART:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	UART	Description
198	UART2_CTS_1V8	UART4_RXD	1.8V	UART4_RX UART2_CTS_B	
1	NC or SD1_DATA3_1V8	SD1_DATA3	1.8V	UART2_RX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
3	NC or SD1_DATA2_1V8	SD1_DATA2	1.8V	UART2_TX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
5	NC or SD1_DATA1_1V8	SD1_DATA1	1.8V	UART1_CTS_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
7	NC or SD1_DATA0_1V8	SD1_DATA0	1.8V	UART1_RTS_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
9	NC or SD1_CMD_1V8	SD1_CMD	1.8V	UART1_RX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
11	NC or SD1_CLK_1V8	SD1_CLK	1.8V	UART1_TX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
18	NC or SAI5_RXC_1V8	SAI3_RXC	1.8V	UART2_CTS_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	UART	Description
21	NC or UART3_RTS_1V8	SD1_RESET_B	1.8V	UART3_RTS_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
22	SD2_CLK	SD2_CLK	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	UART4_RX	
23	NC or UART3_RXD_1V8	SD1_DATA7	1.8V	UART3_RX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
24	SD2_CMD	SD2_CMD	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	UART4_TX	
25	NC or UART3_CTS_1V8	SD1_STROBE	1.8V	UART3_CTS_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
26	SD2_DATA0	SD2_DATA0	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	UART2_RX	
27	NC or UART3_TXD_1V8	SD1_DATA6	1.8V	UART3_TX	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	UART	Description
28	SD2_DATA1	SD2_DATA1	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	UART2_TX	
44	GPIO4_IO21_1V8	SAI2_RXFS	1.8V	UART1_TX	
46	ECSPI1_SSO_1V8	ECSPI1_SSO	1.8V	UART3_RTS_B	
48	ECSPI1_MOSI_1V8	ECSPI1_MOSI	1.8V	UART3_TX	
50	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	UART3_CTS_B	
52	ECSPI1_SCLK_1V8	ECSPI1_SCLK	1.8V	UART3_RX	
94	GPIO4_IO22_1V8	SAI2_RXC	1.8V	UART1_RX	
150	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	UART1_CTS_B	
154	SAI2_RXD_1V8	SAI2_RXDO	1.8V	UART1_RTS_B	
174	UART4_RXD_1V8	ECSPI2_SCLK	1.8V	UART4_RX	
176	UART4_TXD_1V8	ECSPI2_MOSI	1.8V	UART4_TX	
178	UART4_RTS_1V8	ECSPI2_SSO	1.8V	UART4_RTS_B	
180	UART4_CTS_1V8	ECSPI2_MISO	1.8V	UART4_CTS_B	
186	CAN2_TX_1V8	UART3_RXD	1.8V	UART3_RX UART1_CTS_B	
188	CAN2_RX_1V8	UART3_TXD	1.8V	UART3_TX UART1_RTS_B	
192	UART1_RXD_1V8	UART1_RXD	1.8V	UART1_RX	
194	UART1_TXD_1V8	UART1_TXD	1.8V	UART1_TX	
196	UART2_RTS_1V8	UART4_TXD	1.8V	UART4_TX UART2_RTS_B	
198	UART2_CTS_1V8	UART4_RXD	1.8V	UART4_RX UART2_CTS_B	
200	UART2_RXD_1V8	UART2_RXD	1.8V	UART2_RX	
202	UART2_TXD_1V8	UART2_TXD	1.8V	UART2_TX	
206	SAI3_TXC_SOM_1V8	SAI3_TXC		UART2_TX	For SKUs without an Audio Codec only
208	SAI3_TXFS_SOM_1V8	SAI3_TXFS		UART2_RX	For SKUs without an Audio Codec only
210	SAI3_RXD_SOM_1V8	SAI3_RXD		UART2_RTS_B	For SKUs without an Audio Codec only
215	ENET_nRST_1V8	SDA1_DATA4	1.8V	UART2_RTS_B	
217	ENET_nINT_1V8	SD1_DATA5	1.8V	UART2_CTS_B	For SKUs without an on-board Ethernet PHY only

Table 5-17: External Signals of UART

5.18 UNIVERSAL SERIAL BUS (USB)

The USB module is a USB 3.0-compliant serial interface engine for implementing a USB interface. This module is connected to an external port. Collectively the module and external port are the USB 3.0 interface. USB 3.0 supports Super-speed (SS), Highspeed (HS), Full-speed (FS), and Low-speed (LS) operations.

- The upper layer is common for USB 2.0 and USB 3.0 operation. This has the bus interface, buffer management block, list processor for scheduling, and control and status register (CSR) functions.
- USB 2.0 PHY and MAC layers
- USB 3.0 PHY, LINK, and MAC layers

The following table describes the external signals of USB:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USB	Description
130	CSI_MCLK_1V8	GPIO1_IO15	1.8V	USB2_OC	
132	USB1_EN_1V8	GPIO1_IO12	1.8V	USB1_PWR	
134	USB1_OC_1V8	GPIO1_IO13	1.8V	USB1_OC	
136	USB1_VBUS_3V3	USB1_VBUS		USB1_VBUS	USB1 PHY VBUS
138	USB1_ID_1V8	GPIO1_IO10	1.8V	USB1_ID	
140	USB1_D_N	USB1_D_N		USB1_D_N	USB1 PHY data negative
142	USB1_D_P	USB1_D_P		USB1_D_P	USB1 PHY data positive
151	USB2_TX_N	USB2_TX_N		USB2_TX_N	USB2 PHY 3.0 transmit data negative
153	USB2_TX_P	USB2_TX_P		USB2_TX_P	USB2 PHY 3.0 transmit data positive
155	USB2_RX_N	USB2_RX_N		USB2_RX_N	USB2 PHY 3.0 receive data negative
157	USB2_RX_P	USB2_RX_P		USB2_RX_P	USB2 PHY 3.0 receive data positive
161	USB1_TX_N	USB1_TX_N		USB1_TX_N	USB2 PHY 3.0 transmit data negative
163	USB1_TX_P	USB1_TX_P		USB1_TX_P	USB2 PHY 3.0 transmit data positive
165	USB1_RX_N	USB1_RX_N		USB1_RX_N	USB2 PHY 3.0 receive data negative
167	USB1_RX_P	USB1_RX_P		USB1_RX_P	USB2 PHY 3.0 receive data positive
171	USB2_D_N	USB2_D_N		USB2_D_N	USB2 PHY data negative
173	USB2_D_P	USB2_D_P		USB2_D_P	USB2 PHY data positive
175	USB2_EN_1V8	GPIO1_IO14	1.8V	USB2_PWR	
177	USB2_VBUS_3V3	USB2_VBUS		USB2_VBUS	USB2 PHY VBUS
179	USB2_ID_1V8	GPIO1_IO11	1.8V	USB2_ID	

Table 5-18: External Signals of USB

5.19 ULTRA SECURED DIGITAL HOST CONTROLLER (uSDHC)

The Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and the SD/SDIO/MMC cards. The module acts as a bridge, passing host bus transactions to the SD/SDIO/MMC cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC protocols at the transmission level.

The following table describes the external signals of uSDHC:

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USDHC	Description
1	NC or SD1_DATA3_1V8	SD1_DATA3	1.8V	USDHC1_DATA3	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
3	NC or SD1_DATA2_1V8	SD1_DATA2	1.8V	USDHC1_DATA2	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
5	NC or SD1_DATA1_1V8	SD1_DATA1	1.8V	USDHC1_DATA1	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
7	NC or SD1_DATA0_1V8	SD1_DATA0	1.8V	USDHC1_DATA0	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
9	NC or SD1_CMD_1V8	SD1_CMD	1.8V	USDHC1_CMD	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
11	NC or SD1_CLK_1V8	SD1_CLK	1.8V	USDHC1_CLK	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
21	NC or UART3_RTS_1V8	SD1_RESET_B	1.8V	USDHC1_RESET_B	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USDHC	Description
22	SD2_CLK	SD2_CLK	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_CLK	
23	NC or UART3_RXD_1V8	SD1_DATA7	1.8V	USDHC1_DATA7	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
24	SD2_CMD	SD2_CMD	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_CMD	
25	NC or UART3_CTS_1V8	SD1_STROBE	1.8V	USDHC1_STROBE	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
26	SD2_DATA0	SD2_DATA0	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_DATA0	
27	NC or UART3_TXD_1V8	SD1_DATA6	1.8V	USDHC1_DATA6	<p>For SKUs with an on-board WiFi/BT module, this pin is a NC.</p> <p>This pin is only available for SKUs without an on-board WiFi/BT module.</p>
28	SD2_DATA1	SD2_DATA1	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_DATA1	

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USDHC	Description
30	SD2_DATA2	SD2_DATA2	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_DATA2	
32	SD2_DATA3	SD2_DATA3	3.3V or 1.8V Voltage selection through SD_VSEL_1V8 (pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_DATA3	
34	SD2_WP	SD2_WP	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_WP	
36	SD2_nCD	SD2_CD_B	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_CD_B	
38	SD2_RESET_B	SD2_RESET_B	3.3V or 1.8V Voltage selection through SD_VSEL_1V8(pad GPIO1_IO04), 3.3V(SD_VSEL_1V8=Low) 1.8V(SD_VSEL_1V8=High)	USDHC2_RESET_B	
130	CSI_MCLK_1V8	GPIO1_IO15	1.8V	USDHC3_WP	
175	USB2_EN_1V8	GPIO1_IO14	1.8V	USDHC3_CD_B	
179	USB2_ID_1V8	GPIO1_IO11	1.8V	USDHC3_VSELECT	
186	CAN2_TX_1V8	UART3_RXD	1.8V	USDHC3_RESET_B	
188	CAN2_RX_1V8	UART3_TXD	1.8V	USDHC3_VSELECT	
197	PWM_2_1V8	GPIO1_IO09	1.8V	USDHC3_RESET_B	
205	I2C2_SCL_1V8	I2C2_SCL	1.8V	USDHC3_CD_B	
207	I2C2_SDA_1V8	I2C2_SDA	1.8V	USDHC3_WP	
215	ENET_nRST_1V8	SDA1_DATA4	1.8V	USDHC1_DATA4	
217	ENET_nINT_1V8	SD1_DATA5	1.8V	USDHC1_DATA5	For SKUs without an on-board Ethernet PHY only
219	ENET_MIDO_1V8	ENET_MIDO	1.8V	USDHC3_DATA5	For SKUs without an on-board Ethernet PHY only
221	ENET_MDC_1V8	ENET_MDC	1.8V	USDHC3_STROBE	For SKUs without an on-board Ethernet PHY only

Pin No.	VEST i.MX8M Plus SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USDHC	Description
223	NC or ENET_RX_CTL_SOM_1V8	ENET_RX_CTL	1.8V	USDHC3_DATA2	For SKUs without an on-board Ethernet PHY only
225	NC or ENET_RXC_SOM_1V8	ENET_RXC	1.8V	USDHC3_DATA3	For SKUs without an on-board Ethernet PHY only
229	ENET_RDO_SOM_1V8	ENET_RDO	1.8V	USDHC3_DATA4	For SKUs without an on-board Ethernet PHY only
231	ENET_RD1_SOM_1V8	ENET_RD1	1.8V	USDHC3_RESET_B	For SKUs without an on-board Ethernet PHY only
233	ENET_RD2_SOM_1V8	ENET_RD2	1.8V	USDHC3_CLK	For SKUs without an on-board Ethernet PHY only
235	ENET_RX3_SOM_1V8	ENET_RX3	1.8V	USDHC3_CMD	For SKUs without an on-board Ethernet PHY only
237	ENET_TXC_SOM_1V8	ENET_TXC	1.8V	USDHC3_DATA1	For SKUs without an on-board Ethernet PHY only
241	ENET_TX_CTL_SOM_1V8	ENET_TX_CTL	1.8V	USDHC3_DATA0	For SKUs without an on-board Ethernet PHY only
243	ENET_TD0_SOM_1V8	ENET_TXD0	1.8V	USDHC3_WP	For SKUs without an on-board Ethernet PHY only
245	ENET_TD1_SOM_1V8	ENET_TD1	1.8V	USDHC3_CD_B	For SKUs without an on-board Ethernet PHY only
247	ENET_TD2_SOM_1V8	ENET_TD2	1.8V	USDHC3_DATA7	For SKUs without an on-board Ethernet PHY only
249	ENET_TD3_SOM_1V8	ENET_TD3	1.8V	USDHC3_DATA6	For SKUs without an on-board Ethernet PHY only

Table 5-19: External Signals of uSDHC

6 ELECTRICAL SPECIFICATION

6.1 ABSOLUTE MAXIMUM CHARACTERISTICS

Power Supply Input	Minimum	Maximum
Main Power Supply, DC-IN	-0.3	5.5V

Table 6-1: Absolute Maximum Characteristics

6.2 RECOMMENDED POWER SUPPLY CHARACTERISTICS

Power Supply Input	Minimum	Typical	Maximum	Unit
Voltage of Input Power	4.5	5.0	5.5	V
Current of Input Power		TBD		A

Table 6-2: Recommended Power Supply Characteristics

6.3 POWER CONSUMPTION

The VEST i.MX8M Plus SOM power consumption is measured in VEST i.MX8M Plus Carrier Board while running different power scripts under Linux, Yocto.

No.	Power Script	Power Script Operation	I_{max}(A) @ 5.0V Input
1	Power Script 1	LVDS – Play video (H.264) Audio – Headphone in USB – Keyboard and Mouse	TBD
2	Power Script 2	LVDS – Play video (H.264) (foreground) Audio – Headphone in Ethernet – Ping test CPU – Run Stability TEST Utility (background) USB – Keyboard and Mouse	TBD
3	Standby	OS is in idle mode	TBD

Table 6-3: VEST i.MX8M Plus SOM power consumption

Note:

Power consumption is measured on a standard configuration. For customer that require a custom configuration, overall system design and cooling mechanism need to be addressed by the customer.

Layout Recommendations

This chapter provides recommendations to assist design engineers with the correct layout of their VEST i.MX8M Plus SOM based systems.

7.1 VEST i.MX8M PLUS SOM BOARD TRACE LENGTH

Length matching needs to be implemented for each group of high speed signals. The trace lengths of each SOM board signals are listed below. The designer of the carrier board needs to take note of the trace length on the SOM when performing system signals length matching.

Pin No.	Pin Name	Trace Length (Unit: mil)
1	SD1_DATA3_1V8	1708.879
3	SD1_DATA2_1V8	1854.93
5	SD1_DATA1_1V8	1813.869
7	SD1_DATA0_1V8	1741.765
9	SD1_CMD_1V8	1612.843
11	SD1_CLK_1V8	1644.529
13	GND	
15	ONOFF_1V8	1489.495
17	SYS_Nrst_1V8	3869.536
19	SOM_PWR_GOOD_1V8	485.82
21	UART3_RTS_1V8	1578.253
23	UART3_RXD_1V8	1576.219
25	UART3_CTS_1V8	1550.324
27	UART3_TXD_1V8	1388.713
29	GND	
31	LVDS0_TX3_N	907.559
33	LVDS0_TX3_P	904.328
35	LVDS0_TX2_N	848.51
37	LVDS0_TX2_P	847.692
39	GND	
41	LVDS0_CLK_N	782.89
43	LVDS0_CLK_P	780.697
45	GND	
47	LVDS0_TX1_N	724.204
49	LVDS0_TX1_P	726.936
51	LVDS0_TX0_N	677.237
53	LVDS0_TX0_P	674.477
55	GND	
57	LVDS1_TX3_N	623.39
59	LVDS1_TX3_P	622.578
61	LVDS1_TX2_N	564.395
63	LVDS1_TX2_P	564.004
65	GND	
67	LVDS1_CLK_N	504.982
69	LVDS1_CLK_P	502.913
71	GND	
73	LVDS1_TX1_N	486.687
75	LVDS1_TX1_P	487.876
77	LVDS1_TX0_N	475.221
79	LVDS1_TX0_P	472.911
81	GND	

Pin No.	Pin Name	Trace Length (Unit: mil)
2	GND	
4	PWM_4_1V8	2945.813
6	BT_EN_1V8	2841.034
8	WLAN IRQ_1V8	2388.338
10	WLAN_EN_1V8	2404.811
12	SAI5_RXD_1V8	1904.913
14	SAI5_TXD_1V8	1965.372
16	SAI5_RXFS_1V8	2009.394
18	SAI5_RXC_1V8	2043.956
20	GND	
22	SD2_CLK	1357.128
24	SD2_CMD	1353.283
26	SD2_DATA0	1390.58
28	SD2_DATA1	1388.036
30	SD2_DATA2	1496.628
32	SD2_DATA3	1472.083
34	SD2_WP	1487.452
36	SD2_Ncd	1355.205
38	SD2_RESET_B	1270.381
40	GND	
42	GPIO4_IO03_1V8	2057.694
44	GPIO4_IO21_1V8	1959.204
46	ECSPI1_SSO_1V8	1509.141
48	ECSPI1_MOSI_1V8	1581.44
50	ECSPI1_MISO_1V8	1474.122
52	ECSPI1_SCLK_1V8	1446.549
54	GND	
56	EARC_N_HPD	1721.073
58	EARC_P_UTIL	1719.797
60	EARC_AUX	1474.286
62	HDMI_HPD	1392.021
64	HDMI_CEC	1443.787
66	GND	
68	HDMI_TX2_N	1451.888
70	HDMI_TX2_P	1447.745
72	HDMI_TX1_N	1416.378
74	HDMI_TX1_P	1416.481
76	GND	
78	HDMI_TX0_N	1419.488
80	HDMI_TX0_P	1415.87
82	HDMI_TXC_N	1433.29

Pin No.	Pin Name	Trace Length (Unit: mil)
83	CSI2_D0_N	460.029
85	CSI2_D0_P	458.108
87	CSI2_D1_N	454.971
89	CSI2_D1_P	454.15
91	GND	
93	CSI2_CK_N	424.074
95	CSI2_CK_P	424.922
97	GND	
99	CSI2_D2_N	408.559
101	CSI2_D2_P	404.802
103	CSI2_D3_N	399.639
105	CSI2_D3_P	399.272
107	GND	
109	DSI_D3_N	395.435
111	DSI_D3_P	397.579
113	DSI_D2_N	382.084
115	DSI_D2_P	381.218
117	GND	
119	DSI_CK_N	396.157
121	DSI_CK_P	393.417
123	GND	
125	DSI_D1_N	418.786
127	DSI_D1_P	415.562
129	DSI_D0_N	414.967
131	DSI_D0_P	414.55
133	GND	
135	PCIE_TX_N	439.167
137	PCIE_TX_P	439.256
139	PCIE_RX_N	461.61
141	PCIE_RX_P	461.495
143	GND	
145	PCIE_CLK_N	751.001
147	PCIE_CLK_P	751.003
149	GND	
151	USB2_TX_N	630.207
153	USB2_TX_P	627.161
155	USB2_RX_N	645.369
157	USB2_RX_P	642.156
159	GND	
161	USB1_TX_N	634.192
163	USB1_TX_P	632.778
165	USB1_RX_N	655.767
167	USB1_RX_P	655.129
169	GND	
171	USB2_D_N	985.709
173	USB2_D_P	986.561

Pin No.	Pin Name	Trace Length (Unit: mil)
84	HDMI_TXC_P	1431.685
86	GND	
88	HDMI_DDC_SCL	1065.212
90	HDMI_DDC_SDA	1116.48
92	GPIO4_IO00_1V8	1638.695
94	GPIO4_IO22_1V8	1441.426
96	GPIO3_IO22_1V8	1121.54
98	GPIO3_IO23_1V8	1163.205
100	GPIO1_IO05_1V8	971.813
102	GND	
104	CSI1_D3_P	540.407
106	CSI1_D3_N	539.49
108	CSI1_D2_P	522.596
110	CSI1_D2_N	521.247
112	GND	
114	CSI1_CK_P	535.71
116	CSI1_CK_N	534.948
118	GND	
120	CSI1_D1_P	540.816
122	CSI1_D1_N	537.359
124	CSI1_D0_P	548.961
126	CSI1_D0_N	549.892
128	GND	
130	CSI_MCLK_1V8	533.865
132	USB1_EN_1V8	517.72
134	USB1_OC_1V8	544.408
136	USB1_VBUS_3V3	412.359
138	USB1_ID_1V8	526.789
140	USB1_D_N	543.259
142	USB1_D_P	545.897
144	GND	
146	GND	
148	SAI2_MCLK_1V8	1976.799
150	SAI2_TXFS_1V8	1973.6
152	SAI2_TXD_1V8	2006.15
154	SAI2_RXD_1V8	1912.619
156	SAI2_TXC_1V8	1979.878
158	GND	
160	JTAG_TDI_1V8	982.201
162	JTAG_TDO_1V8	920.026
164	JTAG_TMS_1V8	939.917
166	JTAG_TCK_1V8	1010.913
168	JTAG_MOD_1V8	1087.066
170	GPIO4_IO20_1V8	1271.296
172	GND	
174	UART4_RXD_1V8	2462.683

Pin No.	Pin Name	Trace Length (Unit: mil)
175	USB2_EN_1V8	773.662
177	USB2_VBUS_3V3	970.644
179	USB2_ID_1V8	833.641
181	GND	
183	POR_B_1V8	3940.377
185	I2C1_SCL_1V8	3149.068
187	I2C1_SDA_1V8	3521.559
189	HP_DETECT_1V8	1096.445
191	GND	
193	PWM_3_1V8	1455.473
195	PWM_1_1V8	1510.761
197	PWM_2_1V8	976.794
199	GND	
201	I2C4_SCL_1V8	1825.838
203	I2C4_SDA_1V8	1953.464
205	I2C2_SCL_1V8	1962.301
207	I2C2_SDA_1V8	2011.544
209	I2C3_SCL_1V8	2120.699
211	I2C3_SDA_1V8	2034.284
213	GND	
215	ENET_nRST_1V8	2490.902
217	ETH1_LED_ACT	592.82
	ENET_nINT_1V8	3212.394
219	ETH1_LED_10_100	433.715
	ENET_MIDO_1V8	3932.906
221	ETH1_LED_1000	505.255
	ENET_MDC_1V8	3904.89
223	ENET_RX_CTL_SOM_1V8	3208.58
225	ENET_RXC_SOM_1V8	3067.486
227	GND	
229	ETH1_TRX0_P	304.666
	ENET_RDO_SOM_1V8	3471.309
231	ETH1_TRX0_N	309.413
	ENET_RD1_SOM_1V8	3343.455
233	GND	
	ENET_RD2_SOM_1V8	3378.437
235	ETH1_TRX1_P	326.447
	ENET_RX3_SOM_1V8	3306.587
237	ETH1_TRX1_N	326.026
	ENET_TXC_SOM_1V8	2995.173

Pin No.	Pin Name	Trace Length (Unit: mil)
176	UART4_TXD_1V8	2555.323
178	UART4_RTS_1V8	2561.671
180	UART4_CTS_1V8	2295.203
182	CAN1_TX_1V8	1415.416
184	CAN1_RX_1V8	1420.896
186	CAN2_TX_1V8	1192.981
188	CAN2_RX_1V8	1682.301
190	GND	
192	UART1_RXD_1V8	1200.582
194	UART1_TXD_1V8	1721.138
196	UART2_RTS_1V8	1957.013
198	UART2_CTS_1V8	1901.431
200	UART2_RXD_1V8	1315.182
202	UART2_TXD_1V8	1838.008
204	GND	
206	LINE_OUTP	1797.375
	SAI3_TXC_SOM_1V8	2285.554
208	LINE_OUTL	1758.769
	SAI3_TXFS_SOM_1V8	2236.164
210	HP_L	1606.327
	SAI3_RXD_SOM_1V8	2221.182
212	HP_R	1469.984
	SAI3_TXD_SOM_1V8	2301.743
214	MIC_IN	1920.749
	SAI3_MCLK_SOM_1V8	2421.708
216	GND	
	VDD_ETH2	
218	ENET2_RGMII_nINT_1V8	1594.229
220	ENET2_RGMII_MDIO_1V8	2166.376
222	ENET2_RGMII_MDC_1V8	2237.698
224	GND	
226	ENET2_RGMII_RXC_1V8	2744.452
228	ENET2_RGMII_RX_CTL_1V8	1868.418
230	ENET2_RGMII_RDO_1V8	1651.607
232	ENET2_RGMII_RD1_1V8	1727.089
234	ENET2_RGMII_RD2_1V8	2833.828
236	ENET2_RGMII_RD3_1V8	2953.618
238	GND	

Pin No.	Pin Name	Trace Length (Unit: mil)	Pin No.	Pin Name	Trace Length (Unit: mil)
239	GND		240	ENET2_RGMII_TXC_1V8	3080.064
241	ETH1_TRX2_P	319.344	242	ENET2_RGMII_TX_CTL_1V8	3126.967
	ENET_TX_CTL_SOM_1V8	2875.202	244	ENET2_RGMII_TD0_1V8	3104.824
243	ETH1_TRX2_N	316.672	246	ENET2_RGMII_TD1_1V8	3138.131
	ENET_TD0_SOM_1V8	3027.092	248	ENET2_RGMII_TD2_1V8	2826.588
245	GND		250	ENET2_RGMII_TD3_1V8	1952.054
	ENET_TD1_SOM_1V8	3003.529	252	GND	
247	ETH1_TRX3_P	340.559	254	SOM_5V0	
	ENET_TD2_SOM_1V8	3002.842	256	SOM_5V0	
249	ETH1_TRX3_N	339.968	258	SOM_5V0	
	ENET_TD3_SOM_1V8	2955.676	260	SOM_5V0	
251	GND				
253	SOM_5V0				
255	SOM_5V0				
257	SOM_5V0				
259	SOM_5V0				

Table 6-4: Trace Length of SO-DIMM Signals

7.2 PCI EXPRESS INTERFACE RECOMMENDATIONS

Use the following recommendations for PCI Express interface:

- PCIe differential pairs should have a differential impedance of $85\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.
- Match the signals with respect to PCIE_CLK (clock signal) ± 50 mils.

7.3 LVDS RECOMMENDATIONS

Use the following recommendations for the LVDS:

- LVDS differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.
- Match the signals with respect to LVDS_CLK (clock signal) ± 50 mils.

7.4 USB RECOMMENDATIONS

Use the following recommendations for the USB:

- The differential pairs should have a differential impedance of $90\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.

7.5 MIPI CSI RECOMMENDATIONS

Use the following recommendations for the MIPI CSI:

- The differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.

- Match the signals with respect to CSI_CLK (clock signal) $\pm 25\text{mils}$.

7.6 MIPI DSI RECOMMENDATIONS

Use the following recommendations for the MIPI DSI:

- The differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to $\pm 5\text{ mils}$.
- Match the signals with respect to CSI_CLK (clock signal) $\pm 25\text{mils}$.

7.7 SD INTERFACE RECOMMENDATIONS

Use the following recommendations for the SD interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$
- Match the signals with respect to SDx_CLK (clock signal) $\pm 50\text{mils}$.

7.8 SAI RECOMMENDATIONS

Use the following recommendations for the I2S interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$
- Match the signals with respect to clock signal $\pm 100\text{mils}$.

7.9 SPI INTERFACE RECOMMENDATIONS

Use the following recommendations for the SPI interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$
- Match the signals with respect to SPI_CLK (clock signal) $\pm 50\text{mils}$.

7.10 ENET INTERFACE RECOMMENDATIONS

Use the following recommendations for the ENET interface:

- Trace impedance for each differential pair is $100\Omega \pm 10\%$
- Within the differential signals, match the signals $\pm 5\text{mils}$.
- Same pair P/N skew should be less than 20 mils.
- Match the signals with respect to ENET_REF_CLK_50M (clock signal) $\pm 100\text{mils}$.
- The length for each differential pair should be a maximum of 4 inches.

7.11 HDMI RECOMMENDATIONS

Use the following recommendations for the HDMI interface:

- Trace impedance for each differential pair is $100\Omega \pm 10\%$
- Within the differential signals, match the signals $\pm 5\text{mils}$.

Match the signals with respect to HDMI_CLK (clock signal) $\pm 50\text{mils}$.

7 ENVIRONMENTAL SPECIFICATION

7.1 TEMPERATURE SPECIFICATION

The VEST i.MX8M Plus SOM has multiple SKUs with some configurations available with different operating temperatures. For detail, please refer to Section 9 Board Options.

Note: The VEST i.MX8M Plus SOM comes in different operating temperature grade of the SOM components. Nevertheless, customer should consider specific thermal design for the final product and the specific operating environment and operational conditions. Increased temperatures affect the longevity of the parts. Please refer to i.MX 8M Plus product lifetime usage estimates documents mentioned in the Section [2.1](#) specific to your SoC variant for more information.

7.2 HUMIDITY

- Operating: 10% to 90% (Non-condensing)
- Non-operating: 5% to 95% (Non-condensing)

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8 MECHANICAL SPECIFICATION

8.1 MECHANICAL DIMENSION

- $69.6 \times 40 \text{ mm}$

8.2 MECHANICAL DRAWING

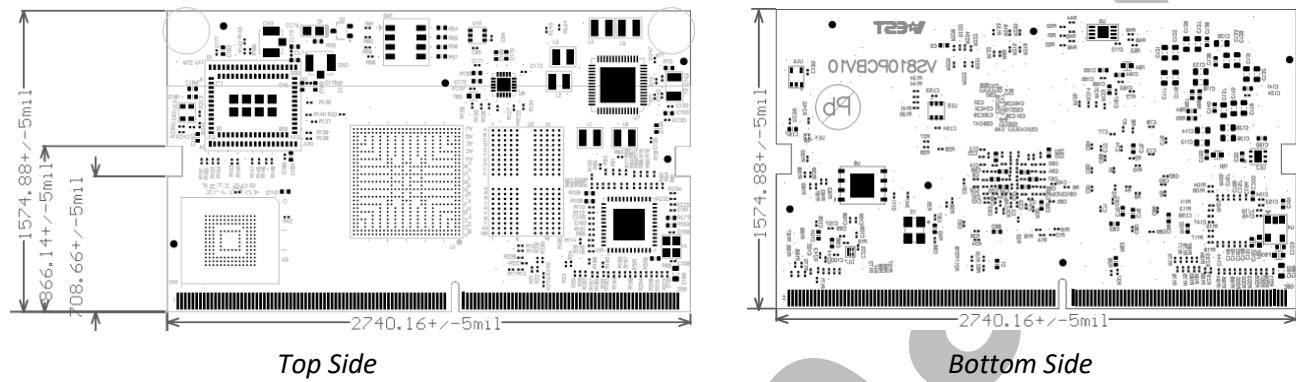


Figure 8-1: Mechanical Drawing

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9 BOARD OPTIONS

(to be update)

Part No.	CPU	CPU Grade	SDRAM	eMMC	Remark

Table 9-1: Board Options and Ordering Part Numbers

More variants of SOM (with Consumer and Industrial Processor options) are available. Please contact your sales representative for more information.

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10 REVISION HISTORY

Version	Date Released	Changes
0.0.1	03/17/2023	<i>Initial Release</i>
B	04/13/2023	<i>Minor updates</i>
C	02/29/2024	<i>Update the board family name from E2I-Plus to VEST i.MX8M Plus</i>

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11 LEGAL NOTICES

The signed agreement between Purchaser and APC will govern the sale and purchase of APC's Venture Embedded Solutions Technology ("VEST") products ("Products"). In the event that no agreement has been concluded, APC's terms and conditions of supply will apply.

Testing and other quality control techniques are used to the extent that APC deems necessary to support its warranty.

Except where required by law, specific testing of all parameters of each Product is not necessarily performed.

Purchaser must provide adequate design and operating safeguards to minimize inherent or procedural and technical risks associated with Purchaser products and applications. Purchaser is solely responsible for its selection and use of APC Products. APC assumes no liability for applications assistance, Purchaser product design or any incompatibility of the Product with Purchaser product.

Products supplied by APC are not designed, intended or authorized for use in life support, life sustaining, medical systems or devices, aircraft navigation, nuclear, or other applications, including, but not limited to, public transportation operating systems, in which the failure of such Products could reasonably be expected to result in personal injury, loss of life or severe property or environmental damage. Purchaser acknowledges that use of APC's Products in such product applications is understood to be fully at the risk of Purchaser and that Purchaser is responsible for verification and validation of the suitability of APC's Products in such applications. Purchaser agrees that APC is not and shall not be liable, in whole or in part, for any claim or damage arising from use in such applications. Purchaser agrees to indemnify, defend and hold APC harmless from and against any and all claims, damages, losses, costs, expenses and liabilities arising out of or in connection with any such use or application.

APC retains all rights to all proprietary intellectual property in the Products and associated manufacturing processes and has the right to file for and obtain intellectual property protection for same.

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