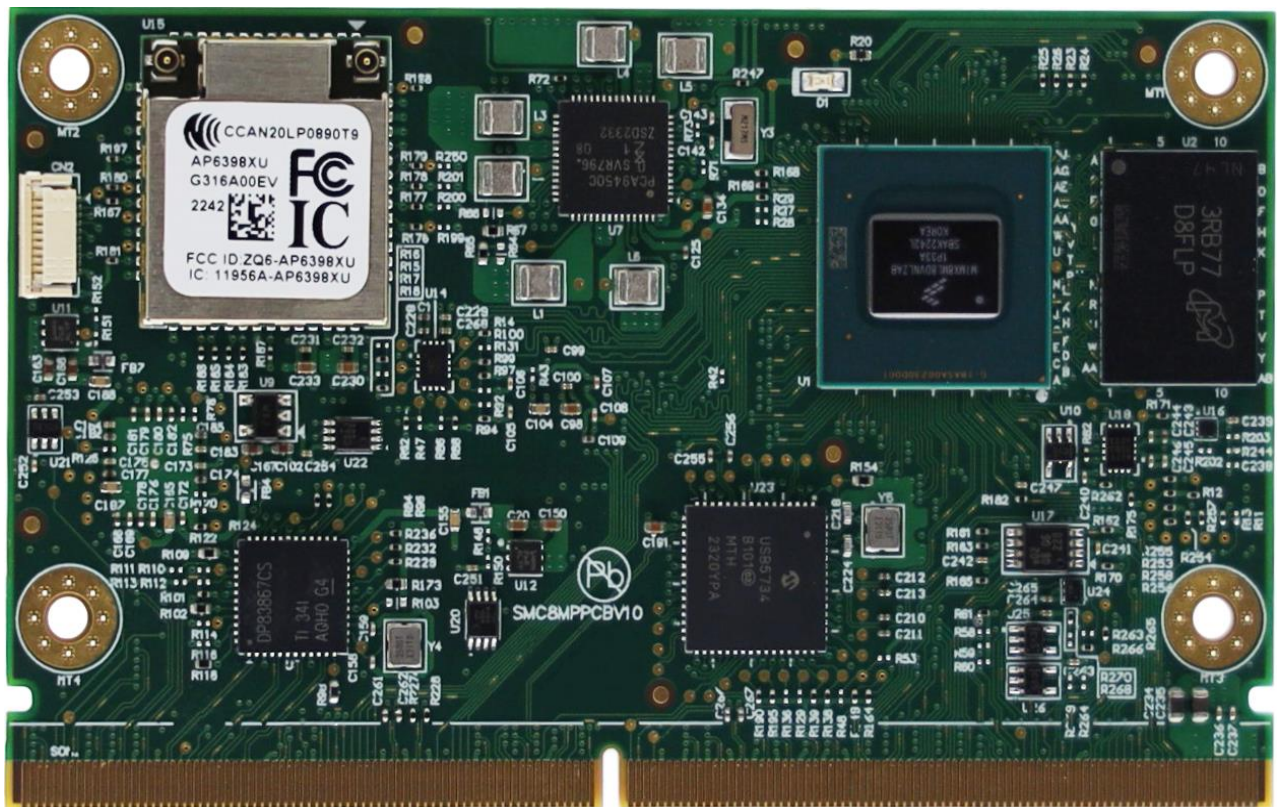


VEST i.MX 8M Plus SMARC SOM Hardware Reference Manual

VEST-i.MX 8M-PLUS-SMARC-SOM-USG-001, REV C



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LIST OF ABBREVIATIONS

Acronyms	Abbreviations
APC	Advanced Products Corporation Private Limited
ARM	Advanced RISC Machine
CAN	Controller Area Network
CSI	Camera Serial Interface
DSI	Display Serial Interface
eCSPI	Enhanced Configurable Serial Peripheral Interface
eMMC	embedded Multi-Media Card (MMC)
GB	Giga Byte
GPIO	General Purpose Input Output
HDMI	High-Definition Multi-media Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
ISO	International Organization for Standardization
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signal
MB	Mega Byte
Mbps	Megabits per second
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
NC	Not Connected
PWM	Pulse Width Modulation
PCIe	Peripheral Component Interconnect Express
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SJC	System JTAG Controller
SOM	System On Module
SOC	System-on-a-Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	Universal Serial Bus on the Go
V*EST	Venture Embedded Solutions Technology "The Logo"
VEST	Venture Embedded Solutions Technology

Table 1-1: List of Abbreviations

REFERENCE DOCUMENTS

- [*i.MX 8M Plus Application Processor Datasheet*](#)
- [*i.MX 8M Plus Application Processor Reference Manual*](#)
- [*i.MX 8M Plus Hardware Developer's Guide*](#)
- [Smart Mobility Architecture \(SMARC\) Hardware Specification](#)
- [Smart Mobility Architecture \(SMARC\) Design Guide](#)

1 OVERVIEW

1.1 GENERAL INFORMATION

The VEST i.MX 8M Plus SMARC SOM (System-On-Module) is based on the NXP's i.MX 8M Plus ARM® Cortex™-A53 processor. The SOM provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics, and video capabilities, as well as high-processing, compact, cost effective and with low power operation.

The VEST i.MX 8M Plus SMARC SOM board runs on the following Operating System:

- Embedded Linux
- Yocto

1.2 FEATURE SUMMARY

- NXP i.MX 8M Plus Processor.
 - ✓ 4x or 2x Cortex-A53 up to 1.8 GHz
 - ✓ Cortex-M7 up to 800 MHz
 - ✓ Neural Processing Unit (NPU): Delivers up to 2.3 TOPS.
 - ✓ Video Decode: 1080p60, h.265/4, VP9, VP8
 - ✓ Video Encode: 1080p60, h.265/4
 - ✓ GPU: 16 GFLOPS (high precision) OpenGL® ES 3.1/3.0, Vulkan®, OpenCL™ 1.2 FP, OpenVG™ 1.1
- Up to 8GB of LPDDR4 SDRAM.
- Up to 256GB eMMC for boot/operating system/application/storage.
- 1x USB 3.0/2.0 Dual-Role with PHY type C
- 2x USB 3.0/2.0 Host
- 2x USB 2.0 Host
- Display: 4-Lane MIPI-DSI, or LVDS (4/8-lane) Tx, HDMI 2.0a Tx
 - ✓ Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.
 - ✓ One LCDIF drives MIPI DSI, up to UWHD and WUXGA
 - ✓ One LCDIF drives LVDS Tx, up to 1920x1080p60.
 - ✓ One LCDIF drives HDMI Tx, up to 4kp30.
- Single Lane PCIe Gen 3
- Up to 2 x SAI
- 1 x SDIO 3.0

- *Up to 5 x I2C*
- *Up to 2 x SPI*
- *Up to 4 x UART*
- *Up to 2 x FlexCAN*
- *Up to 3 x PWM*
- *Two Instances of 4-Lane MIPI CSI*
 - ✓ *With one camera: support up to 12MP@30fps or 4kp45.*
 - ✓ *With two cameras: each supports up to 1080p80.*
- *GPIO*
- *High-Security Cryptographic Device IC (ATECC608, protected storage for up to 16 Keys, Certificates or Data) or on board I2C EEPROM.*
- *2 x on board 10/100/1000 Mbps Ethernet PHY*
- *On board 2.5GHz/5GHz WLAN (IEEE802.11 a/b/g/n/ac), BT 5.0) module*
- *JTAG Connector*
- *3 x Boot SEL*
- *Single 5.0V Input Power Supply*
- *82mm x 50mm Form Factor*
- *314 pin 0.5mm pitch right angle memory socket style connector.*

1.3 BLOCK DIAGRAM

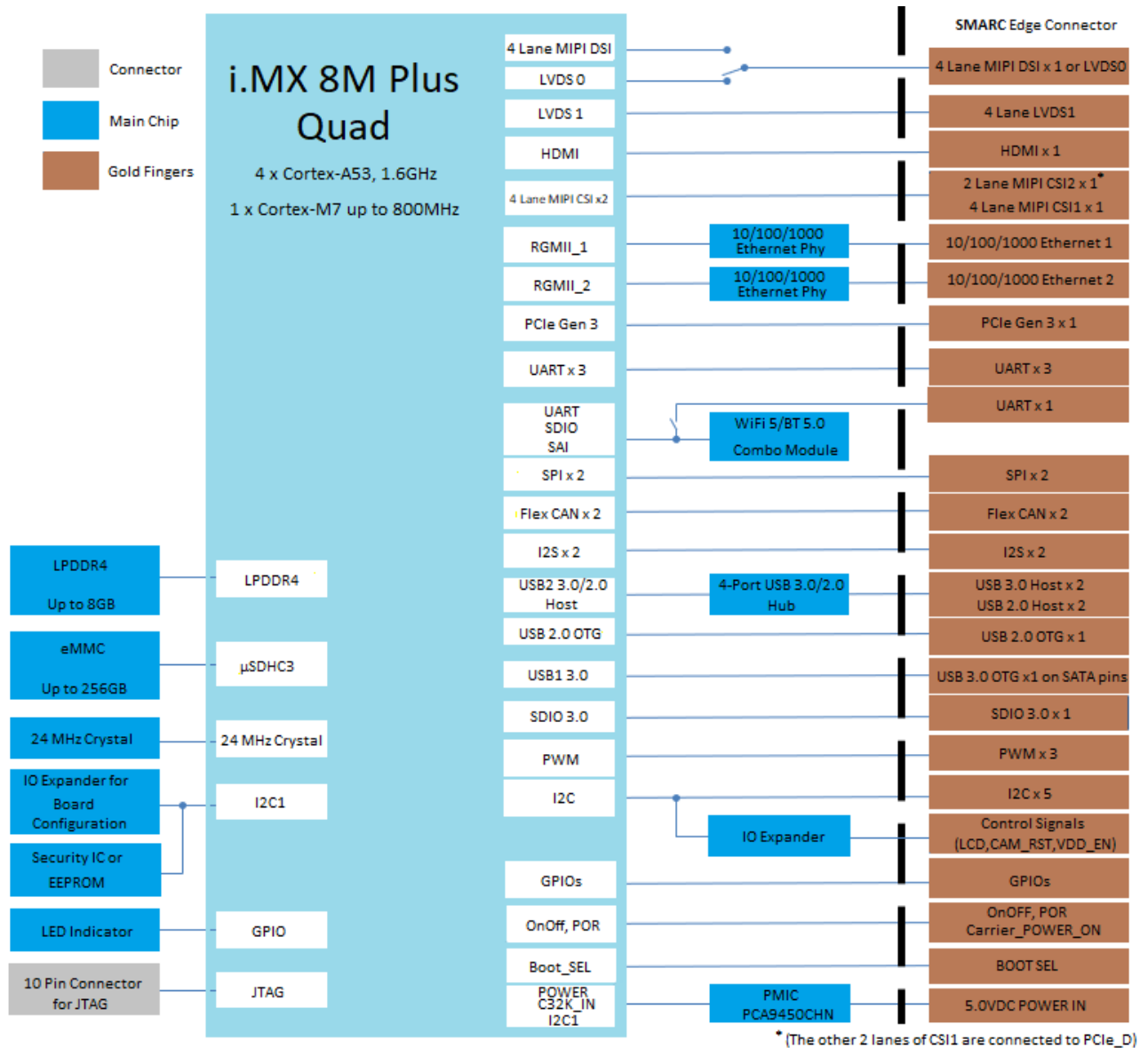


Figure 1-1: VEST i.MX 8M Plus SMARC SOM, Block diagram.

1.4 VEST i.MX 8M PLUS SOM BOARD, CONNECTORS LIST

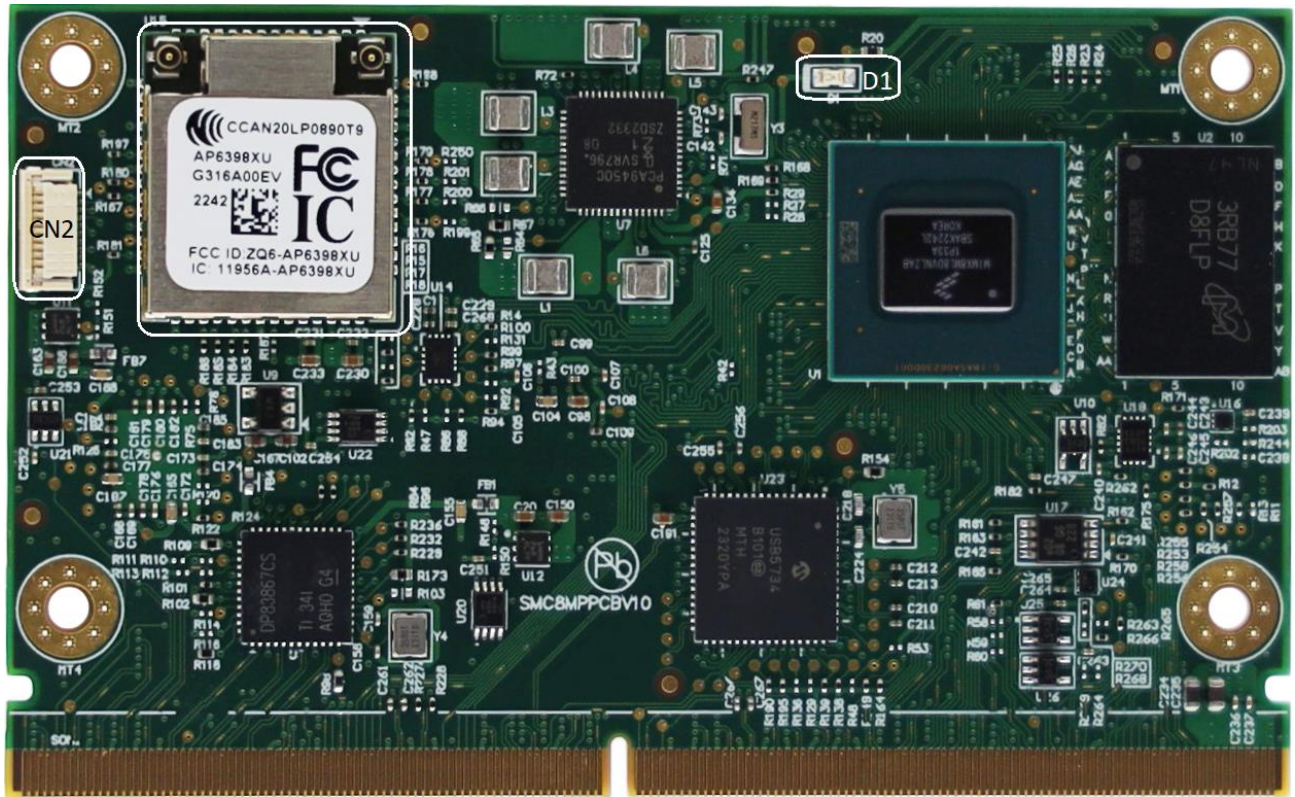


Figure 1-2: VEST i.MX 8M Plus SMARC SOM User Accessible Connector List

The table below lists the user accessible connectors on the VEST i.MX 8M Plus SMARC SOM.

Reference	Function	Type	Pin 1 Location
D1	LED Indicator SYS_STATUS_1V8	Green	
CN2	JTAG	1005 1 9 2 2 - 1 0 1 0 EHLF	
Antenna 1	2.4GHz U.FL RF Antenna Socket	U.FL	
Antenna 2	5GHz U.FL RF Antenna Socket	U.FL	

Table 1-2: VEST i.MX 8M Plus SOM Board User Accessible LED, and Connectors locations

2 MAIN HARDWARE COMPONENTS

This section summarizes the main SMARC SOM hardware building blocks.

2.1 NXP i.MX 8M PLUS

2.1.1 Overview

The i.MX 8M Plus family focuses on machine learning, vision, advanced multimedia, and industrial automation with high reliability. It is built to meet the needs of Smart Home, Building, Smart City, and Industry 4.0 applications.

Powerful quad or dual Arm® Cortex®-A53 processor with a Neural Processing Unit (NPU) operating up to 2.3 TOPS.

Dual image signal processors (ISP) and two camera inputs for an advanced vision system.

The multimedia capabilities include video encode (including h.265) and decode, 3D/2D hardware graphic acceleration, and multiple audio and voice functions.

Real-time control with a Cortex-M7. Robust control networks supported by dual CAN FD and dual Gigabit Ethernet with Time Sensitive Networking (TSN).

High industrial reliability with DRAM inline ECC.

2.1.2 Features

Multicore Processing and Memory Interfaces

- 4x or 2x Cortex-A53 up to 1.8 GHz
- Cortex-M7 up to 800 MHz
- 32-bit DDR4 & LPDDR4 up to 4.0GT/s\

Machine Learning and Vision

- Neural Processing Unit (NPU) that delivers up to 2.3 TOPS.
- Dual Image Signal Processor (ISPs) with resolutions up to 12MP and input rate up to 375MPixels/s
- Camera Interface: 2x MIPI CSI

Advanced Multimedia and Display

- Video Decode: 1080p60, h.265/4, VP9, VP8
- Video Encode: 1080p60, h.265/4.
- GPU: 16 GFLOPS (high precision) OpenGL® ES 3.1/3.0, Vulkan®, Open CL™ 1.2 FP, OpenVG™ 1.1
- Audio: 18x I2S TDM, DSD512, S/PDIF Tx + Rx, 8-ch PDM Mic input, eARC, ASRC
- Low power voice accelerator: Cadence® Tensilica® HiFi 4 DSP @ 800 MHz
- Display: MIPI-DSI, HDMI 2.0a Tx, LVDS (4/8-lane) Tx

High Speed Interfaces

- 2x Gigabit Ethernet with AVB, IEEE 1588, EEE and 1x w/ TSN
- 2x USB 3.0/2.0 Dual-Role with PHY type C

- *PCIe Gen 3*
- *3x SDIO 3.0*
- *2x CAN FD*

Industrial Reliability

- *DDR Inline ECC for LPDDR4 and DDR4*
- *14 FinFET process with low soft error rate (SER)*

Note:

1. Please to refer the latest i.MX 8M Plus datasheet from NXP's website for details.

2.2 10/100/1000MBPS ETHERNET TRANSCEIVER

The SOM features two TI DP83867 single port Gigabit Ethernet PHYs via RGMII interface to the MAC. The DP83867 device is a low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds 8-kV IEC 61000-4-2 (direct contact).

The DP83867 is designed for easy implementation of 10/100/1000 Mbps Ethernet LANs. It interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through Reduced GMII (RGMII) or embedded clock Serial GMII (SGMII).

The DP83867 provides precision clock synchronization, including a synchronous Ethernet clock output. It has low latency and provides IEEE 1588 Start of Frame Detection.

Designed for low power, the DP83867 consumes only 457 mW under full operating power. Wake-on-LAN can be used to further lower the system's power consumption.

The key features supported by the device are:

- *Fully compatible with IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T Specifications.*
- *Exceeds 8000 V IEC 61000-4-2 ESD protection.*
- *Meets EN55011 class B emission standards.*
- *16 programmable RGMII delay modes on RX/TX*
- *Integrated MDI termination resistors*
- *Programmable MAC interface termination impedance*
- *WoL (Wake-on-LAN) packet detection*
- *25-MHz or 125-MHz synchronized clock output*
- *Start of Frame Detect for IEEE 1588 timestamp.*
- *RJ45 mirror mode*
- *Cable diagnostics*
- *Fast link drop mode*

2.3 MEMORY

2.3.1 LPDDR4 SDRAM

The SOM is available with up to 8GB of LPDDR4-4000 SDRAM.

2.3.2 eMMC Flash Memory

The SOM is available with an eMMC Flash Memory with densities up to 256GB. The eMMC flash can be used for Flash Disk, O.S. run-time-image and the Bootloader.

The eMMC is directly connected to i.MX 8M Plus SDHC 3. The eMMC Flash memory is physically located on the bottom side of the SOM.

2.4 ON BOARD SECURITY IC OR I2C EEPROM

The SOM provides High-Security Cryptographic Device IC (ATECC608, with protected storage for up to 16 Keys, Certificates or Data) or on board I2C EEPROM, both share the same footprint and are directly connected to I2C1 bus.

ATECC608B Summary:

The Microchip ATECC608B integrates ECDH (Elliptic Curve Diffie Hellman) an ultra-secure security protocol to provide key agreement for encryption/decryption, along with ECDSA (Elliptic Curve Digital Signature Algorithm) sign-verify authentication for the Internet of Things (IoT) market including home automation, industrial networking, medical, as well as accessories and consumables authentication and more. Additionally, the ATECC608B offers an integrated AES hardware accelerator strengthening hardware-based security for LoRaWAN applications and enable secure boot capabilities for very small microcontrollers.

2.5 FOUR PORT USB SS/HI-SPEED HUB

The SOM features a four port Hi-Speed Hub. The Hub also supports Full Speed and Low Speed USB signaling for offering complete coverage of all defined USB operating speeds.

2.6 PMIC

The SOM uses NXP PCA9450CHN Power Management IC. The PCA9450 is a single chip PMIC specifically designed to support i.MX 8M family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5 V adapter for nonportable applications.

The device provides six high-efficiency step-down regulators, five LDOs, one 400 mA load switch, 2 channel level translator, a 32.768 kHz crystal oscillator driver, and buck regulators. The buck regulators support dynamic voltage scaling (DVS) with programmable ramping up and down times and remote sensing to compensate for IR drop to the load.

2.7 ON BOARD WLAN AND BLUETOOTH MODULE

The SOM is configured with a Dual Band WiFi 802.11 a/b/g/b/ac 2 x 2 MIMO + Bluetooth 5.2 Module.

3 EXTERNAL INTERFACE

The VEST i.MX 8M Plus SMARC SOM has a 314-pin edge connector with gold fingers that mates with a low profile 314 pin 0.5mm pitch right angle connector.

Note:

The i.MX 8M Plus contains a limited number of pins, most of which have multiple signal options that are muxed. These signal to pin, and pin to signal options, are selected by the input-output multiplexer called the IOMUX.

Below Pin assignments, a list of the pad names of the chip, the various signals that can be assigned to each of the pads, for more details please refer to the latest i.MX 8M Plus datasheet.

Pin Number: Pin Number of the VEST i.MX 8M Plus SMARC SOM PCB edge connector.

SMARC Pin Name: Pin name of the VEST i.MX 8M Plus SMARC SOM PCB edge connector.

Signal Name: Signal name of the i.MX 8M Plus.

Signal Type: Signal type of this pin

Voltage Level: Voltage level of this pin

Description: Brief pin functionality description

The following Table describes the pinout of the VEST i.MX 8M Plus SMARC SOM PCB edge connector.

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
P1	SMB_ALERT#	SMB_ALERT#_1V8	I	1V8	SMBus Alert Signal active low
P2	GND	GND	Ground	Ground	Ground
P3	CSI1_CK+	CSI1_CK_P	I	Differential	CSI1 Differential Clock+
P4	CSI1_CK-	CSI1_CK_N	I	Differential	CSI1 Differential Clock-
P5	GBE1_SDP	ENET1_CLKI25_3V3	O	3V3	IEEE 1588 Trigger Signal for Hardware Implementation of Precision Time Protocol (PTP)
P6	GBE0_SDP	ENET0_CLKI25_3V3	O	3V3	IEEE 1588 Trigger Signal for Hardware Implementation of Precision Time Protocol (PTP)
P7	CSI1_RX0+	CSI1_D0_P	I	Differential	CSI1_RX0+ Differential input
P8	CSI1_RX0-	CSI1_D0_N	I	Differential	CSI1_RX0- Differential input
P9	GND	GND	Ground	Ground	Ground
P10	CSI1_RX1+	CSI1_D1_P	I	Differential	CSI1_RX1+ Differential input
P11	CSI1_RX1-	CSI1_D1_N	I	Differential	CSI1_RX1- Differential input
P12	GND	GND	Ground	Ground	Ground
P13	CSI1_RX2+	CSI1_D2_P	I	Differential	CSI1_RX2+ Differential input
P14	CSI1_RX2-	CSI1_D2_N	I	Differential	CSI1_RX2- Differential input
P15	GND	GND	Ground	Ground	Ground
P16	CSI1_RX3+	CSI1_D3_P	I	Differential	CSI1_RX3+ Differential input
P17	CSI1_RX3-	CSI1_D3_N	I	Differential	CSI1_RX3- Differential input
P18	GND	GND	Ground	Ground	Ground
P19	GBE0_MDI3-	ETH0_TRX3_N	I/O	Differential	Gigabit Ethernet 0 MDI3+
P20	GBE0_MDI3+	ETH0_TRX3_P	I/O	Differential	Gigabit Ethernet 0 MDI3-
P21	GBE0_LINK100#	ETH0_LED_10_100_3V3_OD	O OD	3V3	Link Speed Indication 100 Mbps
P22	GBE0_LINK1000#	ETH0_LED_1000_3V3_OD	O OD	3V3	Link Speed Indication 1000 Mbps
P23	GBE0_MDI2-	ETH0_TRX2_N	I/O	Differential	Gigabit Ethernet 0 MDI2+
P24	GBE0_MDI2+	ETH0_TRX2_P	I/O	Differential	Gigabit Ethernet 0 MDI2-
P25	GBE0_LINK_ACT#	ETH0_LED_ACT_3V3_OD	O OD	3V3	Link Activity Indication
P26	GBE0_MDI1-	ETH0_TRX1_N	I/O	Differential	Gigabit Ethernet 0 MDI1+

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
P27	GBE0_MDI1+	ETH0_TRX1_P	I/O	Differential	Gigabit Ethernet 0 MDI1-
P28	GBE0_CTREF	NC	-		No Connection
P29	GBE0_MDIO-	ETH0_TRX0_N	I/O	Differential	Gigabit Ethernet 0 MDIO+
P30	GBE0_MDIO+	ETH0_TRX0_P	I/O	Differential	Gigabit Ethernet 0 MDIO-
P31	SPIO_CS1#	NC	-		No Connection
P32	GND	GND	Ground	Ground	Ground
P33	SDIO_WP	SD2_WP	I	1V8/3V3	Input State of Write Protect Tab
P34	SDIO_CMD	SD2_CMD	I/O	1V8/3V3	SDIO Command/Response
P35	SDIO_CD#	SD2_nCD	I	1V8/3V3	SDIO Card Detect
P36	SDIO_CLK	SD2_CLK	O	1V8/3V3	SDIO Clock
P37	SDIO_PWR_EN	SD2_RESET_B	O	1V8/3V3	SDIO Power Enable
P38	GND	GND	Ground	Ground	Ground
P39	SDIO_D0	SD2_DATA0	I/O	1V8/3V3	SDIO Data 0
P40	SDIO_D1	SD2_DATA1	I/O	1V8/3V3	SDIO Data 1
P41	SDIO_D2	SD2_DATA2	I/O	1V8/3V3	SDIO Data 2
P42	SDIO_D3	SD2_DATA3	I/O	1V8/3V3	SDIO Data 3
P43	SPIO_CS0#	ECSP11_SSO_1V8	O	1V8	SPIO Master Chip Select 0
P44	SPIO_CLK	ECSP11_SCLK_1V8	O	1V8	SPIO Clock
P45	SPIO_DIN	ECSP11_MISO_1V8	I	1V8	SPIO Master input/ Slave output
P46	SPIO_DO	ECSP11_MOSI_1V8	O	1V8	SPIO Master output/ Slave input
P47	GND	GND	Ground	Ground	Ground
P48	SATA_TX+	USB1_TX_P*	O	Differential	SMARC exception, USB0 SuperSpeed Transmit+
P49	SATA_TX-	USB1_TX_N*	O	Differential	SMARC exception, USB0 SuperSpeed Transmit-
P50	GND	GND	Ground	Ground	Ground
P51	SATA_RX+	USB1_RX_P*	I	Differential	SMARC exception, USB0 SuperSpeed Receive+
P52	SATA_RX-	USB1_RX_N*	I	Differential	SMARC exception, USB0 SuperSpeed Receive-
P53	GND	GND	Ground	Ground	Ground
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	ECSP12_SSO_1V8	O	1V8	SPI1 Master Chips Select 0
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	NC	-		No Connection
P56	ESPI_CLK / SPI1_CLK / QSPI_CLK	ECSP12_SCLK_1V8	O	1V8	SPI1 Clock
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	ECSP12_MISO_1V8	I/O	1V8	SPI1 Master input/ Slave output
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	ECSP12_MOSI_1V8	I/O	1V8	SPI1 Master output/ Slave input
P59	GND	GND	Ground	Ground	Ground
P60	USB0+	USB1_D_P	I/O	Differential	USB0 Data+
P61	USB0-	USB1_D_N	I/O	Differential	USB0 Data-
P62	USB0_EN_OC#	USB1_EN_OC#_3V3	I/O	3V3	USB0 Over Current
P63	USB0_VBUS_DET	USB1_VBUS_5V0	I	5V0	USB0 Host VBUS 5V0
P64	USB0_OTG_ID	USB1_ID_1V8	I	1V8	USB0 OTG Device Detect
P65	USB1+	USB_DN1_D_P	I/O	Differential	USB1 DATA+
P66	USB1-	USB_DN1_D_N	I/O	Differential	USB1 DATA-
P67	USB1_EN_OC#	USB_DN1_OC#_3V3	I/O	3V3	USB1 Over Current
P68	GND	GND	Ground	Ground	Ground
P69	USB2+	USB_DN2_D_P	I/O	Differential	USB2 DATA+
P70	USB2-	USB_DN2_D_N	I/O	Differential	USB2 DATA-
P71	USB2_EN_OC#	USB_DN2_EN_OC#_3V3	I/O	3V3	USB2 Over-Current
P72	RSVD	NC	-		No Connection
P73	RSVD	NC	-		No Connection
P74	USB3_EN_OC#	USB_DN3_EN_OC#_3V3	I/O	3V3	USB3 Over-Current
Key					
P75	PCIE_A_RST#	PCIE_RST#_3V3	O	3V3	PCie Port A Reset Output
P76	USB4_EN_OC#	USB_DN4_EN_OC#_3V3	I/O	3V3	USB4 Over-Current
P77	PCIE_B_CLKREQ#	NC	-		No Connection
P78	PCIE_A_CLKREQ#	PCI_CLKREQ_B_3V3_OD	I/O OD	3V3	PCie Port A Clock Request
P79	GND	GND	Ground	Ground	Ground
P80	PCIE_C_REFCK+	NC	-		No Connection
P81	PCIE_C_REFCK-	NC	-		No Connection
P82	GND	GND	Ground	Ground	Ground
P83	PCIE_A_REFCK+	PCIE_CLK_P	I/O	Differential	PCie Reference Clock+ Link A
P84	PCIE_A_REFCK-	PCIE_CLK_N	I/O	Differential	PCie Reference Clock- Link A
P85	GND	GND	Ground	Ground	Ground
P86	PCIE_A_RX+	PCIE_RX_P	I	Differential	PCie link Data+ Receive Link A
P87	PCIE_A_RX-	PCIE_RX_N	I	Differential	PCie link Data- Receive Link A
P88	GND	GND	Ground	Ground	Ground
P89	PCIE_A_TX+	PCIE_TX_P	O	Differential	PCie link Data+ Transmit Link A
P90	PCIE_A_TX-	PCIE_TX_N	O	Differential	PCie link Data- Transmit Link A
P91	GND	GND	Ground	Ground	Ground

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P	O	Differential	HDMI Differential Data D2+
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX2_N	O	Differential	HDMI Differential Data D2-
P94	GND	GND	Ground	Ground	Ground
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P	O	Differential	HDMI Differential Data D1+
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX1_N	O	Differential	HDMI Differential Data D1-
P97	GND	GND	Ground	Ground	Ground
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P	O	Differential	HDMI Differential Data D0+
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX0_N	O	Differential	HDMI Differential Data D0-
P100	GND	GND	Ground	Ground	Ground
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TXC_P	O	Differential	HDMI Differential Clock+
P102	HDMI_CK- / DP1_LANE3-	HDMI_TXC_N	O	Differential	HDMI Differential Clock-
P103	GND	GND	Ground	Ground	Ground
P104	HDMI_HPD / DP1_HPD	HDMI_HPD_1V8	I	1V8	HDMI Hot Plug detect
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL_1V8	I/O OD	1V8	DDC Clock for HDMI
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA_1V8	I/O OD	1V8	DDC Data for HDMI
P107	DP1_AUX_SEL	NC	-		No Connection
P108	GPIO0 / CAM0_PWR#	CAM0_PWR#_1V8	O	1V8	Camera 0 Power Enable, Active Low
P109	GPIO1 / CAM1_PWR#	CAM1_PWR#_1V8	O	1V8	Camera 1 Power Enable, Active Low
P110	GPIO2 / CAM0_RST#	CAM0_RST#_1V8	O	1V8	Camera 0 Reset, Active Low
P111	GPIO3 / CAM1_RST#	CAM1_RST#_1V8	O	1V8	Camera 1 Reset, Active Low
P112	GPIO4 / HDA_RST#	GPIO4_1V8	I/O	1V8	GPIO4 / HDA_RST#
P113	GPIO5 / PWM_OUT	PWM_1_1V8	I/O	1V8	GPIO5 / PWM Out
P114	GPIO6 / TACHIN	GPIO6_1V8	I/O	1V8	I2C Touch INT
P115	GPIO7	GPIO7_1V8	I/O	1V8	GPIO7
P116	GPIO8	GPIO8_1V8	I/O	1V8	GPIO8
P117	GPIO9	GPIO9_1V8	I/O	1V8	GPIO9
P118	GPIO10	GPIO10_1V8	I/O	1V8	GPIO10
P119	GPIO11	GPIO11_1V8	I/O	1V8	GPIO11
P120	GND	GND	Ground	Ground	Ground
P121	I2C_PM_CK	I2C1_SCL_1V8	I/O I/O	1V8	Power Management I2C bus Clock
P122	I2C_PM_DAT	I2C1_SDA_1V8	I/O I/O	1V8	Power Management I2C bus Data
P123	BOOT_SEL0#	BOOT_MODE0_1V8	I	1V8	Boot Select bit 0
P124	BOOT_SEL1#	BOOT_MODE1_1V8	I	1V8	Boot Select bit 1
P125	BOOT_SEL2#	BOOT_MODE2_1V8	I	1V8	Boot Select bit 2
P126	RESET_OUT#	RESET_OUT#_1V8	O	1V8	General purpose Reset to Carrier Board
P127	RESET_IN#	RESET_IN_1V8	I OD	1V8	Reset input from Carrier Board
P128	POWER_BTN#	POWER_BTN	I OD	1V8	Power Button input from carrier board
P129	SER0_TX	UART4_TXD_1V8	O	1V8	UART4 Transmit
P130	SER0_RX	UART4_RXD_1V8	I	1V8	UART4 Receive
P131	SER0_RTS#	UART4_CTS_1V8	O	1V8	UART4 Clear to Send
P132	SER0_CTS#	UART4_RTS_1V8	I	1V8	UART4 Request to Send
P133	GND	GND	Ground	Ground	Ground
P134	SER1_TX	UART1_TXD_1V8	O	1V8	UART1 Transmit
P135	SER1_RX	UART1_RXD_1V8	I	1V8	UART1 Receive
P136	SER2_TX	UART2_TXD_1V8*	O	1V8	UART2 Transmit, shared with on board WiFi/BT module, default is WiFi/BT
P137	SER2_RX	UART2_RXD_1V8*	I	1V8	UART2 Receive, shared with on board WiFi/BT module, default is WiFi/BT
P138	SER2_RTS#	UART2_CTS_1V8*	O	1V8	UART2 Request to Send, shared with on board WiFi/BT module, default is WiFi/BT
P139	SER2_CTS#	UART2_RTS_1V8*	I	1V8	UART2 Clear to Send, shared with on board WiFi/BT module, default is WiFi/BT
P140	SER3_TX	UART3_TXD_1V8	O	1V8	UART3 Transmit
P141	SER3_RX	UART3_RXD_1V8	I	1V8	UART3 Receive
P142	GND	GND	Ground	Ground	Ground
P143	CAN0_TX	CAN1_TX_1V8	O	1V8	CAN Port 0 Transmit
P144	CAN0_RX	CAN1_RX_1V8	I	1V8	CAN Port 0 Receive
P145	CAN1_TX	CAN2_TX_1V8	O	1V8	CAN Port 1 Transmit
P146	CAN1_RX	CAN2_RX_1V8	I	1V8	CAN Port 1 Receive
P147	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P148	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P149	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P150	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P151	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P152	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P153	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P154	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P155	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
P156	VDD_IN	VSYS_5V0	VDD 5V0	5V0	Power input VDD 5V0
S1	CSI1_TX+ / I2C_CAM1_CK	I2C2_SCL_1V8	I/O OD	1V8	I2C Serial Clock Camera 1
S2	CSI1_TX- / I2C_CAM1_DAT	I2C2_SDA_1V8	I/O OD	1V8	I2C Serial Data Camera 1

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
S3	GND	GND	Ground	Ground	Ground
S4	RSVD	NC	-		No Connection
S5	CSIO_TX+ / I2C_CAM0_CK	I2C5_SCL_1V8	I/O OD	1V8	I2C Serial Data Camera 0
S6	CAM_MCK	CSI_MCLK_1V8	O	1V8	Master Clock Output
S7	CSIO_TX- / I2C_CAM0_DAT	I2C5_SDA_1V8	I/O OD	1V8	I2C Serial Clock Camera 0
S8	CSIO_CK+	CSI2_CK_P	I	Differential	CSIO Clock+
S9	CSIO_CK-	CSI2_CK_N	I	Differential	CSIO Clock-
S10	GND	GND	Ground	Ground	Ground
S11	CSIO_RX0+	CSI2_D0_P	I	Differential	CSIO_RX0+ Differential Data
S12	CSIO_RX0-	CSI2_D0_N	I	Differential	CSIO_RX0- Differential Data
S13	GND	GND	Ground	Ground	Ground
S14	CSIO_RX1+	CSI2_D1_P	I	Differential	CSIO_RX1+ Differential Data
S15	CSIO_RX1-	CSI2_D1_N	I	Differential	CSIO_RX1- Differential Data
S16	GND	GND	Ground	Ground	Ground
S17	GBE1_MDIO+	ETH1_TRX0_P	I/O	Differential	Gigabit Ethernet 1 MDIO+
S18	GBE1_MDIO-	ETH1_TRX0_N	I/O	Differential	Gigabit Ethernet 1 MDIO-
S19	GBE1_LINK100#	ETH1_LED_10_100_3V3_OD	O OD	3V3	Link Speed Indication for 100 Mbps
S20	GBE1_MD1+	ETH1_TRX1_P	I/O	Differential	Gigabit Ethernet 1 MD1+
S21	GBE1_MD1-	ETH1_TRX1_N	I/O	Differential	Gigabit Ethernet 1 MD1-
S22	GBE1_LINK1000#	ETH1_LED_1000_3V3_OD	O OD	3V3	Link Speed Indication for 1000 Mbps
S23	GBE1_MD12+	ETH1_TRX2_P	I/O	Differential	Gigabit Ethernet 1 MD12+
S24	GBE1_MD12-	ETH1_TRX2_N	I/O	Differential	Gigabit Ethernet 1 MD12-
S25	GND	GND	Ground	Ground	Ground
S26	GBE1_MD13+	ETH1_TRX3_P	I/O	Differential	Gigabit Ethernet 1 MD13+
S27	GBE1_MD13-	ETH1_TRX3_N	I/O	Differential	Gigabit Ethernet 1 MD13-
S28	GBE1_CTREF	NC	-		No Connection
S29	PCIE_D_TX+ / SERDES_O_TX+	CSI2_D2_P*	O	Differential	SMARC exception, CSIO RX2+ Differential Data
S30	PCIE_D_TX- / SERDES_O_TX-	CSI2_D2_N*	O	Differential	SMARC exception, CSI1 RX2- Differential Data
S31	GBE1_LINK_ACT#	ETH1_LED_ACT*_3V3_OD	O	3V3	Link Activity Indication
S32	PCIE_D_RX+ / SERDES_O_RX+	CSI2_D3_P*	I	Differential	SMARC exception, CSIO RX3+ Differential Data
S33	PCIE_D_RX- / SERDES_O_RX-	CSI2_D3_N*	I	Differential	SMARC exception, CSIO RX3- Differential Data
S34	GND	GND	Ground	Ground	Ground
S35	USB4+	USB4_DN4_D_P	I/O	Differential	USB Data+ Port 4
S36	USB4-	USB4_DN4_D_N	I/O	Differential	USB Data- Port 4
S37	USB3_VBUS_DET	NC	-		No Connection
S38	AUDIO_MCK	SAI2_MCLK_1V8	O	1V8	Master Clock Output to I2S Codec
S39	I2S0_LRCK	SAI2_TXFS_1V8	I/O	1V8	I2S0 Left and Right Synchronization clock
S40	I2S0_SDOUT	SAI2_TXD_1V8	O	1V8	I2S0 Digital Audio Output
S41	I2S0_SDIN	SAI2_RXD_1V8	I	1V8	I2S0 Digital Audio Input
S42	I2S0_CK	SAI2_TXC_1V8	I/O	1V8	I2S0 Digital Audio Clock
S43	ESPI_ALERT0#	NC	-		No Connection
S44	ESPI_ALERT1#	NC	-		No Connection
S45	MDIO_CLK	NC	-		No Connection
S46	MDIO_DAT	NC	-		No Connection
S47	GND	GND	Ground	Ground	Ground
S48	I2C_GP_CK	I2C4_SCL_1V8	I/O	1V8	General Purpose I2C Clock
S49	I2C_GP_DAT	I2C4_SDA_1V8	I/O	1V8	General Purpose I2C Data
S50	HDA_SYNC / I2S2_LRCK	SAI3_TXFS_1V8	I/O	1V8	I2S2 Left and Right Synchronization Clock
S51	HDA_SDO / I2S2_SDOUT	SAI3_TXD_1V8	O	1V8	I2S2 Digital Audio Output
S52	HDA_SDI / I2S2_SDIN	SAI3_RXD_1V8	I/O	1V8	I2S2 Digital Audio Input
S53	HDA_CK / I2S2_CK	SAI3_TXC_1V8	O	1V8	I2S2 Digital Audio Clock
S54	SATA_ACT#	NC	-		No Connection
S55	USB5_EN_OC#	NC	-		No Connection
S56	ESPI_IO_2 / QSPI_IO_2	NC	-		No Connection
S57	ESPI_IO_3 / QSPI_IO_3	NC	-		No Connection
S58	ESPI_RESET#	NC	-		No Connection
S59	USB5+	NC	-		No Connection
S60	USB5-	NC	-		No Connection
S61	GND	GND	Ground	Ground	Ground
S62	USB3_SSTX+	USB_DN3_SSTX_P	O	Differential	USB SuperSpeed Transmit+ Port 3
S63	USB3_SSTX-	USB_DN3_SSTX_N	O	Differential	USB SuperSpeed Transmit- Port 3
S64	GND	GND	Ground	Ground	Ground
S65	USB3_SSRX+	USB_DN3_SSRX_P	I	Differential	USB SuperSpeed Receive+ Port 3
S66	USB3_SSRX-	USB_DN3_SSRX_N	I	Differential	USB SuperSpeed Receive- Port 3
S67	GND	GND	Ground	Ground	Ground
S68	USB3+	USB_DN3_D_P	I/O	Differential	USB3 Data+ Port 3
S69	USB3-	USB_DN3_D_N	I/O	Differential	USB3 Data- Port 3
S70	GND	GND	Ground	Ground	Ground
S71	USB2_SSTX+	USB_DN2_SSTX_P	O	Differential	USB SuperSpeed Transmit+ Port 2

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
S72	USB2_SSTX-	USB_DN2_SSTX_N	O	Differential	USB SuperSpeed Transmit- Port 2
S73	GND	GND	Ground	Ground	Ground
S74	USB2_SSRX+	USB_DN2_SSRX_P	I	Differential	USB SuperSpeed Receive+ Port 2
S75	USB2_SSRX-	USB_DN2_SSRX_N	I	Differential	USB SuperSpeed Receive- Port 2
S76	PCIE_B_RST#	NC	-		No Connection
Key					
S77	PCIE_C_RST#	NC	-		No Connection
S78	PCIE_C_RX+ / SERDES_1_RX+	EARC_N_HPD	I/O	1V8	SMARC exception, EARC_N_HPD
S79	PCIE_C_RX- / SERDES_1_RX-	EARC_P_UTIL	I/O	1V8	SMARC exception, EARC_N_UTIL
S80	GND	GND	Ground	Ground	Ground
S81	PCIE_C_TX+ / SERDES_1_TX+	EARC_AUX	I/O	1V8	SMARC exception, EARC_AUX
S82	PCIE_C_TX- / SERDES_1_TX-	EHDMI_CEC	I/O	1V8	SMARC exception, HDMI_CEC
S83	GND	GND	Ground	Ground	Ground
S84	PCIE_B_REFCK+	NC	-		No Connection
S85	PCIE_B_REFCK-	NC	-		No Connection
S86	GND	GND	Ground	Ground	Ground
S87	PCIE_B_RX+	NC	-		No Connection
S88	PCIE_B_RX-	NC	-		No Connection
S89	GND	GND	Ground	Ground	Ground
S90	PCIE_B_TX+	NC	-		No Connection
S91	PCIE_B_TX-	NC	-		No Connection
S92	GND	GND	Ground	Ground	Ground
S93	DPO_LANE0+	NC	-		No Connection
S94	DPO_LANE0-	NC	-		No Connection
S95	DPO_AUX_SEL	NC	-		No Connection
S96	DPO_LANE1+	NC	-		No Connection
S97	DPO_LANE1-	NC	-		No Connection
S98	DPO_HPD	NC	-		No Connection
S99	DPO_LANE2+	NC	-		No Connection
S100	DPO_LANE2-	NC	-		No Connection
S101	GND	GND	Ground	Ground	Ground
S102	DPO_LANE3+	NC	-		No Connection
S103	DPO_LANE3-	NC	-		No Connection
S104	USB3_OTG_ID	NC	-		No Connection
S105	DPO_AUX+	NC	-		No Connection
S106	DPO_AUX-	NC	-		No Connection
S107	LCD1_BKLT_EN	LVDS1_BKLT_EN_1V8	O	1V8	LCD1 Backlight Enable
S108	LVDS1_CLK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	I/O	Differential	LVDS1 Differential Clock+
S109	LVDS1_CLK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	I/O	Differential	LVDS1 Differential Clock-
S110	GND	GND	Ground	Ground	Ground
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_TX0_P	O	Differential	LVDS1 Differential Data D0+
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_TX0_N	O	Differential	LVDS1 Differential Data D0-
S113	eDP1_HPD / DSI1_TE	NC	-		No Connection
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_TX1_P	O	Differential	LVDS1 Differential Data D0+
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_TX1_N	O	Differential	LVDS1 Differential Data D0-
S116	LCD1_VDD_EN	LVDS1_VDD_EN_1V8	O	1V8	LCD1 VDD Enable
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_TX2_P	O	Differential	LVDS1 Differential Data D2+
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_TX2_N	O	Differential	LVDS1 Differential Data D2-
S119	GND	GND	Ground	Ground	Ground
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_TX3_P	O	Differential	LVDS1 Differential Data D3+
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_TX3_N	O	Differential	LVDS1 Differential Data D3-
S122	LCD1_BKLT_PWM	PWM_3_1V8	O	1V8	LCD1 PWM Backlight Control
S123	GPIO13	GPIO13_1V8	I/O	1V8	GPIO13
S124	GND	GND	Ground	Ground	Ground
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_DSI0_TX0_P	O	Differential	LVDS0, DSI0+ Differential Data D0+, default is LVDS
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_DSI0_TX0_N	O	Differential	LVDS0, DSI0- Differential Data D0-, default is LVDS
S127	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_BKLT_EN_1V8	O	1V8	LVDS0, DSI0 Backlight Enable
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_DSI0_TX1_P	O	Differential	LVDS0, DSI0+ Differential Data D1+, default is LVDS
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_DSI0_TX1_N	O	Differential	LVDS0, DSI0- Differential Data D1-, default is LVDS
S130	GND	GND	Ground	Ground	Ground
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_TX2_P	O	Differential	LVDS0, DSI0+ Differential Data D2+, default is LVDS
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_TX2_N	O	Differential	LVDS0, DSI0- Differential Data D2-, default is LVDS

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Description
S133	LCD0_VDD_EN	LVDS0_VDD_EN_1V8	O	1V8	LCD0 VDD Enable
S134	LVDS0_CK+ / eDP0_AUX+ /DSIO_CLK+	LVDS0_DSIO_CLK_P	O	Differential	LVDS0, DSIO+ Differential Clock+, default is LVDS
S135	LVDS0_CK- / eDP0_AUX- /DSIO_CLK-	LVDS0_DSIO_CLK_N	O	Differential	LVDS0, DSIO- Differential Clock-, default is LVDS
S136	GND	GND	Ground	Ground	Ground
S137	LVDS0_3+ / eDP0_TX3+ / DSIO_D3+	LVDS0_DSIO_TX3_P	O	Differential	LVDS0, DSIO+ Differential Data D3+, default is LVDS
S138	LVDS0_3- / eDP0_TX3- / DSIO_D3-	LVDS0_DSIO_TX3_N	O	Differential	LVDS0, DSIO- Differential Data D3-, default is LVDS
S139	I2C_LCD_CK	I2C3_SCL_1V8	I/O	1V8	DDC Clock
S140	I2C_LCD_DAT	I2C3_SDA_1V8	I/O	1V8	DDC Data Line
S141	LCD0_BKLT_PWM	LCD0_PWM2_1V8	O	1V8	LCD0 PWM Brightness Control
S142	GPIO12	GPIO12_1V8	I/O	1V8	GPIO12
S143	GND	GND	Ground	Ground	Ground
S144	eDP0_HPDP / DSIO_TE	NC	-		No Connection
S145	WDT_TIME_OUT#	WDOG_B_1V8	O	1V8	Watch Dog Timer Output active low
S146	PCIE_WAKE#	PCIE_WAKE#_3V3	I	3V3	PCIE Wakeup interrupt to Links A, B, C, D
S147	VDD_RTC	NC	-		No Connection
S148	LID#	LID#_1V8	I	1V8	Lid Open/Close
S149	SLEEP#	SLEEP#_1V8	I	1V8	Sleep indicator from Carrier board
S150	VIN_PWR_BAD#	VIN_PWR_BAD#_1V8	I	1V8	Voltage in Power Bad on Carrier Board
S151	CHARGING#	CHARGING#_1V8	I	1V8	Charging
S152	CHARGER_PRSENT#	CHARGER_PRSENT#_1V8	I	1V8	Charger Present
S153	CARRIER_STBY#	CARRIER_STBY#_1V8	O	1V8	Carrier Standby
S154	CARRIER_PWR_ON	CARRIER_PWR_ON_1V8	O	1V8	Carrier Power On
S155	FORCE_RECOV#	FORCE_RECOV#_1V8	I	1V8	Force recover
S156	BATLOW#	BATLOW#_1V8	I	1V8	Battery low indication to Module
S157	TEST#	NC	-		No Connection
S158	GND	GND	GROUND	GROUND	GROUND

Table 3-1 i.MX 8M SMARC SOM Connector

3.1 JTAG (CN2)

The following table describes the external signals of the JTAG:

Pin No.	Signal Name	Signal Type	Voltage Level	Description
1	VDD_JTAG	Power	1V8	VDD JTAG
2	JTAG_TRST#	I	1V8	JTAG POWER ON RESET active low
3	JTAG_TMS	O	1V8	JTAG TMS
4	JTAG_TDO	O	1V8	JTAG TDO
5	JTAG_TDI	I	1V8	JTAG TDI
6	JTAG_TCK	O	1V8	JTAG TCK
7	NC	NC	-	No Connection
8	JTAG_RESET_IN#	I	1V8	JTAG Reset input active low
9	MFG_MODE#	O	1V8	MFG Mode active low
10	GND	GND	GND	Ground
S1	GND	GND	GND	Ground
S2	GND	GND	GND	Ground

Table 3-2 JTAG Connection to Carrier Board (CN2)

4 SIGNAL DESCRIPTION PER BLOCK/INSTANCE

This chapter describes in detail the default SOM pins, the pin names, and the external interfaces per block/instance.

Pin Number:	Pin Number of the VEST i.MX 8M Plus SMARC SOM PCB edge connector.
SMARC Pin Name:	Pin name of the VEST i.MX 8M Plus SMARC SOM PCB edge connector.
Signal Name:	Signal name of the i.MX 8M Plus.
Signal Type:	Signal type of this pin
Voltage Level:	Voltage level of this pin
Description:	Brief pin functionality description

5.1 CLOCK CONTROLLER MODULE (CCM)

The Clock Control Module (CCM) manages the on-chip module clocks. CCM receives clocks from PSSs and oscillators and creates clocks for the on-chip peripherals through a set of multiplexers, dividers, and gates. When entering or exiting a low power mode, the CCM automatically turns on and off PLLs and peripheral clocks.

The following table describes the external signals of CCM:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	Signal Type	Signal
S152	PWM_3_1V8	GPIO1_IO14	1.8V	O	CCM_CLKO1
P57	ECSPI2_MISO_1V8	ECSPI2_MISO	1.8V	O	
S6	CSI_MCLK_1V8	GPIO1_IO15	1.8V	O	CCM_CLKO2
P54	ECSPI2_SS0_1V8	ECSPI2_SS0	1.8V	O	

Table 4-1: External Signals of CCM

5.2 ENHANCED CONFIGURABLE SPI (ECSPI)

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block.

The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO). The ECSP's data FIFOs allow rapid data communication with fewer software interrupts.

The following table describes the external signals of ECSPI:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	Signal	Description
P43	ECSPI1_SS0_1V8	ECSPI1_SS0	1.8V	ECSPI1_SS0	Chip select signal
P46	ECSPI1_MOSI_1V8	ECSPI1_MOSI	1.8V	ECSPI1_MOSI	Master data out; slave data in
P45	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	ECSPI1_MISO	Master data in; slave data out
P44	ECSPI1_SCLK_1V8	ECSPI1_SCLK	1.8V	ECSPI1_SCLK	SPI clock signal
P56	ECSPI2_SCLK_1V8	ECSPI2_SCLK	1.8V	ECSPI2_SCLK	SPI clock signal

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	Signal	Description
P36	SD2_CLK	SD2_CLK	1.8V	ECSPI1_MOSI	Master data out; slave data in
P58	ECSPI2_MOSI_1V8	ECSPI2_MOSI	1.8V	ECSPI2_MOSI	Master data out; slave data in
P34	SD2_CMD	SD2_CMD	1.8V	ECSPI1_SCLK	SPI clock signal
P54	ECSPI2_SS0_1V8	ECSPI2_SS0	1.8V	ECSPI2_SS0	Chip select signal
P41	SD2_DATA2	SD2_DATA2	1.8V	ECSPI2_MOSI	Master data out; slave data in
P57	ECSPI2_MISO_1V8	ECSPI2_MISO	1.8V	ECSPI2_MISO	Master data in; slave data out
P42	SD2_DATA3	SD2_DATA3	1.8V	ECSPI2_MISO	Master data in; slave data out
P135	UART1_RXD_1V8	UART1_RXD	1.8V	ECSPI3_SCLK	SPI clock signal
P134	UART1_TXD_1V8	UART1_TXD	1.8V	ECSPI3_MOSI	Master data out; slave data in
P130	UART2_RXD_1V8_SOM	UART2_RXD	1.8V	ECSPI3_MISO	Master data in; slave data out, shared UART2 pin with on board WiFi/BT
P129	UART2_TXD_1V8	UART2_TXD	1V8	ECSP13_SS0	Chip select signal shared with UART2 pin with on board WiFi/BT

Table 4-2: External Signals of ECSPI

5.3 FLEXIBLE CONTROLLER AREA NETWORK (FLEXCAN)

The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

The CAN protocol was originally designed to be used as a vehicle serial data bus, meeting the specific real-time processing and reliable operation requirements in the EMI environment of a vehicle. The FlexCAN module is a full implementation of the CAN protocol specification. The CAN with the Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, that support both standard and extended message frames and long payloads.

The following table describes the external signals of FLEXCAN:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	FLEXCAN
P143	CAN1_TX_1V8	SAI2_RXC	1.8V	CAN1_TX
P105	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	CAN1_TX
S42	SAI2_TXC_1V8	SAI2_TXC	1.8V	CAN1_RX
P144	CAN1_RX_1V8	SPDIF_RX	1.8V	CAN1_RX
P106	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	CAN1_RX
S40	SAI2_TXD_1V8	SAI2_TXD0	1.8V	CAN2_TX
P145	CAN2_TX_1V8	UART3_RXD	1.8V	CAN2_TX
S38	SAI2_MCLK_1V8	SAI2_MCLK	1.8V	CAN2_RX
P104	HDMI_HPD	HDMI_HPD	1.8V	CAN2_RX
P146	CAN2_RX_1V8	UART3_TXD	1.8V	CAN2_RX

Table 4-3: External Signals of FLEXCAN

5.4 HDMI

HDMI (c2.0a) can transfer uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25MHz up to 297MHz. HDMI can support several audio standards. It can support up to eight IEC60958 L-PCM audio channels, including IEC61937 compressed non-linear PCM and HBR (high bit rate) audio interfaces. HDMI has the capability of automatically setting the display's format configuration (intelligent link).

The following table describes the external signals of HDMI.

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	HDMI
P95	HDMI_TX1_P	HDMI_TX1_P	Differential	HDMI_TX1_P
P104	HDMI_HPD	HDMI_HPD	1.8V	HDMI_HPD/HDMI_HPD_O
P93	HDMI_TX2_N	HDMI_TX2_N	Differential	HDMI_TX2_N
P92	HDMI_TX2_P	HDMI_TX2_P	Differential	HDMI_TX2_P
P90	HDMI_TX1_N	HDMI_TX1_N	Differential	HDMI_TX1_N
P99	HDMI_TX0_N	HDMI_TX0_N	Differential	HDMI_TX0_N
P98	HDMI_TX0_P	HDMI_TX0_P	Differential	HDMI_TX0_P
P102	HDMI_TXC_N	HDMI_TXC_N	Differential	HDMI_TXC_N
P101	HDMI_TXC_P	HDMI_TXC_P	Differential	HDMI_TXC_P
P105	HDMI_DDC_SCL	HDMI_DDC_SCL	1.8V	HDMI_SCL
P106	HDMI_DDC_SDA	HDMI_DDC_SDA	1.8V	HDMI_SDA

Table 4-4: External Signals of HDMI

5.5 LVDS DISPLAY BRIDGE (LDB)

This chip supports one LVDS Tx display and Pixel Mapper. The LVDS port may be used as follows:

- Single channel (4 lanes) supports resolutions up to 720p60.
- Dual asynchronous channels (8 data, 2 clocks)
 - Supports resolutions up to 1920x1200p60.
 - Intended for a single panel with two interfaces, when transferring across two channels (even pixel/odd pixel).
 - The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream.

The following table describes the external signals of LVDS:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	LVDS
S138	LVDS0_TX3_N	LVDS0_D3_N	LVDS0_D3_N
S137	LVDS0_TX3_P	LVDS0_D3_P	LVDS0_D3_P
S132	LVDS0_TX2_N	LVDS0_D2_N	LVDS0_D2_N
S131	LVDS0_TX2_P	LVDS0_D2_P	LVDS0_D2_P
S135	LVDS0_CLK_N	LVDS0_CLK_N	LVDS0_CLK_N

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	LVDS
S134	LVDS0_CLK_P	LVDS0_CLK_P	LVDS0_CLK_P
S129	LVDS0_TX1_N	LVDS0_D1_N	LVDS0_D1_N
S128	LVDS0_TX1_P	LVDS0_D1_P	LVDS0_D1_P
S126	LVDS0_TX0_N	LVDS0_D0_N	LVDS0_D0_N
S125	LVDS0_TX0_P	LVDS0_D0_P	LVDS0_D0_P
S121	LVDS1_TX3_N	LVDS1_D3_N	LVDS1_D3_N
S118	LVDS1_TX2_N	LVDS1_D2_N	LVDS1_D2_N
S120	LVDS1_TX3_P	LVDS1_D3_P	LVDS1_D3_P
S109	LVDS1_CLK_N	LVDS1_CLK_N	LVDS1_CLK_N
S108	LVDS1_CLK_P	LVDS1_CLK_P	LVDS1_CLK_P
S117	LVDS1_TX2_P	LVDS1_D2_P	LVDS1_D2_P
S115	LVDS1_TX1_N	LVDS1_D1_N	LVDS1_D1_N
S114	LVDS1_TX1_P	LVDS1_D1_P	LVDS1_D1_P
S112	LVDS1_TX0_N	LVDS1_D0_N	LVDS1_D0_N
S111	LVDS1_TX0_P	LVDS1_D0_P	LVDS1_D0_P

Table 4-5: External Signals of LVDS

5.6 MIPI- CAMERA SERIAL INTERFACE HOST CONTROLLER (MIPI_CSI)

The MIPI Camera Serial Interface (MIPI_CSI2) works with MIPI DPHY module to connect to the host processor.

MIPI_CSI2 supports RAW, YUV and RGB image formats when used in conjunction with an output to ISI (Image Sensing Interface) or ISP (Image Signal Processing).

The chip supports two 4-lane MIPI CSI2 camera inputs. The key features of the MIPI CSI2 (controller and PHY) include:

- Compliant to MIPI-CSI2 standard
- Support up to 4 data lanes
- When one ISP is used, MIPI CSI interface 1 supports:
 - Pixel clock up to 400MHz at nominal voltage and 500MHz at overdrive voltage
 - 80Mbps - 1.5Gbps per lane data rate in high speed operation
- When two ISPs are used, both MIPI CSI interfaces support:
 - Pixel clock up to 266MHz at nominal and overdrive voltage
 - 80Mbps - 1.5Gbps per lane data rate in high speed operation (the maximum speed of 1.5Gbps per lane is only supported when only 2 data lanes are used)
- When used in conjunction an ISP output, the RAW8, RAW10, RAW12, and RAW14 image formats are supported
- When used in conjunction with an ISI output, the YUV420 (8-bit and 10-bit), YUV422 (8-bit and 10-bit), RGB565, RGB666, RGB888 image formats are supported
- Support for a 10Mbps data rate in low power operation

The following table describes the external signals of MIPI_CSI:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	MIPI_CSI
S12	CSI2_D0_N	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N
S11	CSI2_D0_P	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P
S15	CSI2_D1_N	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N
S14	CSI2_D1_P	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P
S9	CSI2_CLK_N	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N
S8	CSI2_CLK_P	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P
S30*	CSI2_D2_N	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N
S29*	CSI2_D2_P	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P
S33*	CSI2_D3_N	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N
S32*	CSI1_D3_P	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P
P16	CSI2_D3_P	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P
P17	CSI1_D3_N	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N
P13	CSI1_D2_P	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P
P14	CSI1_D2_N	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N
P3	CSI1_CLK_P	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N
P4	CSI1_CLK_N	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P
P10	CSI1_D1_P	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P
P11	CSI1_D1_N	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N
P7	CSI1_D0_P	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P
P8	CSI1_D0_N	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N

Table 4-6: External Signals of MIPI_CSI

5.7 MIPI- DISPLAY SERIAL INTERFACE HOST CONTROLLER (MIPI_DSI)

MIPI Display Serial Interface (DSI) is a flexible, high-performance core that allows communication with MIPI DSI compliant peripherals.

This chip supports one 4-lane MIPI DSI display with pixels from the LCDIF. The key features of the MIPI DSI (controller and PHY) include:

- Compliant to MIPI-DSI standard v1.2
- Supports up to 4 data lanes
- Maximum resolution limited to resolutions achievable with a 250MHz pixel clock and active pixel rate of 200Mpixel/s with 24-bit RGB. This includes resolutions show below:
 - 1080 p60
 - WUXGA (1920x1200) at 60 Hz
 - 1920x1440 at 60 Hz
 - UWHD (2560x1080) at 60 Hz
 - WQHD (2560x1440) can be supported in a reduced blanking mode
- Supports 80Mbps - 1.5Gbps data rate in high speed operation
- Supports 10Mbps data rate in low power operation

The following table describes the external signals of MIPI_DSI:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	MIPI_DSI
S138	DSI_D3_N	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N
S137	DSI_D3_P	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P
S132	DSI_D2_N	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N
S131	DSI_D2_P	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P
S135	DSI_CLK_N	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N
S134	DSI_CLK_P	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P
S129	DSI_D1_N	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N
S128	DSI_D1_P	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P
S126	DSI_D0_N	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N
S125	DSI_D0_P	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P

Table 4-7: External Signals of MIPI_DSI

5.8 PCI EXPRESS (PCIe)

The PCIe PHY IP core is used for PCI-Express (PCIe) applications. The transceiver in the core performs the following functions:

- Serializes the 8b/10b encoded data for transmission for Gen1 and Gen2 operation, and 128b/130b encoded data for Gen3
- De-serializes the received code groups

When transmitting the data, the transceiver performs these functions:

- Accepts four 10-bit 8b/10b encoded transmit characters or four 8-bit 128b/130b encoded data
- Attaches and serializes the data to the TXP/TXN differential outputs to a maximum value of 8.0 Gb/s

When receiving the data, the transceiver performs these functions:

- Samples the received serial data on the RXP/RXN differential inputs
- Deserializes it into four 10-bit(or 8b-bit) received characters

PCIe PHY core has on-chip PLL circuitry for synthesis of the baud-rate transmitter clocks, and extraction of the retimed clocks from the received serial stream.

The following table describes the external signals of PCIe:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	PCIe
P90	PCIe_TX_N	PCIe_TXN_N	PCIe1_TXN_N
P89	PCIe_TX_P	PCIe_TXN_P	PCIe1_TXN_P
P87	PCIe_RX_N	PCIe_RXN_N	PCIe1_RXN_N
P86	PCIe_RX_P	PCIe_RXN_P	PCIe1_RXN_P
P84	PCIe_CLK_N	PCIe_REF_PAD_CLK_N	PCIe1_REF_PAD_CLK_N
P83	PCIe_CLK_P	PCIe_REF_PAD_CLK_P	PCIe1_REF_PAD_CLK_P
P78	PCI_CLKREQ_B_3V3_OD	UART4_RXD	PCIe1_CLKREQ_B

Table 4-8: External Signals of PCIe

5.9 PDM MICROPHONE INTERFACE (PDM)

The Pulse Density Modulated Microphone Interface is a common way to deliver audio from microphones to a processor in several applications such as mobile telephones. However, current digital-audio systems use multibit audio signal (also known as multibit PCM) to represent the signal. This block implements the required digital interface to provide a 24-bits audio signal from a PDM microphone bitstream in a configurable output sampling rate.

The implementation of this digital interface is based on the application of hardware digital signal processing techniques. The PDM Microphone Interface architecture was designed to save gate count and minimize

power consumption. It implements a series of filters to transform a PDM bitstream to a 24-bit PCM audio signal.

The whole module is designed to work in multichannel mode. All channels have the same configuration, but each input channel can be turned on/off independently.

The following table describes the external signals of PDM:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PDM
P34	SD2_CMD	SD2_CMD	1.8V	PDM_CLK
P119	GPIO11_1V8	SAI5_RXC	1.8V	PDM_CLK
P110	CAM0_RST#_1V8	SAI3_RXC	1.8V	PDM_CLK
S107	LVDS1_BKLT_EN_1V8	SAI1_RXC	1.8V	PDM_CLK
P39	SD2_DATA0	SD2_DATA0	1.8V	PDM_BIT_STREAM0
P40	SD2_DATA1	SD2_DATA1	1.8V	PDM_BIT_STREAM1
S42	SAI2_TXC_1V8	SAI2_TXC	1.8V	PDM_BIT_STREAM1
S52	SAI3_RXD_1V8	SAI3_RXD	1.8V	PDM_BIT_STREAM1
S133	LVDS0_VDD_EN_1V8	SAI1_RXD1	1.8V	PDM_BIT_STREAM1
P143	CAN1_TX_1V8	SAI2_RXC	1.8V	PDM_BIT_STREAM1
S39	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	PDM_BIT_STREAM2
P41	SD2_DATA2	SD2_DATA2	1.8V	PDM_BIT_STREAM2
S53	SAI3_TXC_1V8	SAI3_TXC	1.8V	PDM_BIT_STREAM2
S123	GPIO13	SAI2_RXFS	1.8V	PDM_BIT_STREAM2
S41	SAI2_RXD_1V8	SAI2_RXD0	1.8V	PDM_BIT_STREAM3
P42	SD2_DATA3	SD2_DATA3	1.8V	PDM_BIT_STREAM3

Table 4-9: External Signals of PDM

5.10 PULSE WIDTH MODULATION (PWM)

The Pulse Width Modulation (PWM) has a 16-bit counter, and it is optimized to generate sound from stored sampled audio images. It uses 16-bit resolution and a 4 x 16 data FIFO.

The following features characterize the PWM:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configurable output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

The following table describes the external signals of PWM:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	PWM
S7	I2C4_SDA_1V8	I2C4_SDA	1.8V	PWM1_OUT
P113	PWM_1_1V8	SPDIF_EXT_CLK	1.8V	PWM1_OUT
S140	I2C5_SDA_1V8	SAI5_MCLK	1.8V	PWM1_OUT
S5	I2C4_SCL_1V8	I2C4_SCL	1.8V	PWM2_OUT
S141	PWM_2_1V8	GPIO1_IO09	1.8V	PWM2_OUT
P144	CAN1_RX_1V8	SPDIF_RX	1.8V	PWM2_OUT
S2	I2C3_SDA_1V8	I2C3_SDA	1.8V	PWM3_OUT
P64	USB1_ID_1V8	GPIO1_IO10	1.8V	PWM3_OUT
S122	PWM_3_1V8	GPIO1_IO14	1.8V	PWM3_OUT
S139	I2C5_SCL_1V8	SPDIF_TX	1.8V	PWM3_OUT
P119	GPIO11_1V8	SAI5_RXC	1.8V	PWM3_OUT
S139	I2C3_SCL_1V8	I2C3_SCL	1.8V	PWM4_OUT
S6	CSI_MCLK_1V8	GPIO1_IO15	1.8V	PWM4_OUT
S142	GPIO12_1V8	SAI3_MCLK	1.8V	PWM4_OUT

Table 4-10: External Signals of PWM

5.11 SYNCHRONOUS AUDIO INTERFACE (SAI)

The Synchronous Audio Interface (SAI) provides full-duplex serial interfaces with frame synchronization formats such as I2S, AC97, TDM, and codec/DSP interfaces.

The following table describes the external signals of SAI:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	SAI
S38	SAI2_MCLK_1V8	SAI2_MCLK	1.8V	SAI2_MCLK/SAI5_MCLK/SAI3_MCLK
S39	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	SAI2_TX_SYNC/SAI5_TX_DATA1/SAI2_TX_DATA1
S40	SAI2_TXD_1V8	SAI2_TXD0	1.8V	SAI2_TX_DATA0/SAI5_TX_DATA3
S41	SAI2_RXD_1V8	SAI2_RXD0	1.8V	SAI2_RX_DATA0/SAI5_TX_DATA0/SAI2_TX_DATA1
S42	SAI2_TXC_1V8	SAI2_TXC	1.8V	SAI2_TX_BCLK/SAI5_TX_DATA2
S53	SAI3_TXC_1V8	SAI3_TXC	1.8V	SAI3_TX_BCLK/SAI2_TX_DATA2/SAI5_RX_DATA2
S50	SAI3_TXFS_1V8	SAI3_TXFS	1.8V	SAI3_TX_SYNC/SAI2_TX_DATA1/SAI5_RX_DATA1/SAI3_TX_DATA 1
S52	SAI3_RXD_1V8	SAI3_RXD	1.8V	SAI3_RX_DATA0/SAI2_RX_DATA3/SAI5_RX_DATA0
S51	SAI3_TXD_1V8	SAI3_TXD	1.8V	SAI3_TX_DATA0/SAI2_TX_DATA3/SAI5_RX_DATA3

Table 4-11: External Signals of SAI

5.12 SPDIF

SPDIF supports raw capture mode that can save all incoming bits into an audio buffer.

SPDIF Receiver: Support for 32kHz - 192kHz sample rate

SPDIF Transmitter: Support for 32kHz - 192kHz data transmit rate.

The following table describes the external signals of SPDIF:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name*	iMX8M Plus Pad Name	Voltage Level	SPDIF
P41	SD2_DATA2	SD2_DATA2	1.8V	SPDIF1_OUT
P139	I2C5_SCL_1V8	SPDIF_TX	1.8V	SPDIF1_OUT
S142	GPIO12_1V8	SAI3_MCLK	1.8V	SPDIF1_OUT SPDIF1_IN
P42	SD2_DATA3	SD2_DATA3	1.8V	SPDIF1_IN
P144	CAN1_RX_1V8	SPDIF_RX	1.8V	SPDIF1_IN
P113	PWM_1_1V8	SPDIF_EXT_CLK	1.8V	SPDIF1_EXT_CLK
S51	SAI3_TXD_1V8	SAI3_TXD	1.8V	SPDIF1_EXT_CLK

Table 4-12: External Signals of SPDIF

*Note: The SMARC specification does not support SPDIF and does not have SPDIF pins. The SPDIF outputs from the iMX-8M Plus have been repurposed.

5.13 UART

The Universal Asynchronous Receiver/Transmitter (UART) provides serial communication capability with external devices through a level converter and an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.

The UART supports NRZ encoding format, RS485 compatible 9-bit data format and IrDA-compatible infrared slow data rate (SIR) format.

The following table describes the external signals of UART:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	UART
P134	UART1_TXD_1V8	UART1_TXD	1.8V	UART1_TX
P112	GPIO4_1V8	SAI2_RXFS	1.8V	UART1_TX
P143	CAN1_TX_1V8	SAI2_RXC	1.8V	UART1_RX
P135	UART1_RXD_1V8	UART1_RXD	1.8V	UART1_RX
S39	SAI2_TXFS_1V8	SAI2_TXFS	1.8V	UART1_CTS_B
S41	SAI2_RXD_1V8	SAI2_RXD0	1.8V	UART1_RTS_B
P40	SD2_DATA1	SD2_DATA1	1.8V	UART2_TX
P136*	NC or UART2_TXD_1V8	UART2_TXD	1.8V	UART2_TX
P137*	NC or UART2_RXD_1V8	UART2_RXD	1.8V	UART2_RX
P139*	NC or UART2_RTS_1V8	SD1_DATA4	1.8V	UART2_RTS_B
P138*	NC or UART2_CTS_1V8	SD1_DATA5	1.8V	UART2_CTS_B
P109	CAM1_PWR#_1V8	SD1_RESET_B	1.8V	UART3_RTS_B
P36	SD2_CLK	SD2_CLK	1.8V	UART4_RX
P141	UART3_RXD_1V8	SD1_DATA7	1.8V	UART3_RX
P44	ECSP11_SCLK_1V8	ECSP11_SCLK	1.8V	UART3_RX
P34	SD2_CMD	SD2_CMD	1.8V	UART4_TX

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	UART
P111	CAM1_RST#_1V8	SD1_STROBE	1.8V	UART3_CTS_B
P140	UART3_TXD_1V8	SD1_DATA6	1.8V	UART3_TX
P46	ECSPI1_MOSI_1V8	ECSPI1_MOSI	1.8V	UART3_TX
P145	CAN2_TX_1V8	UART3_RXD	1.8V	UART3_RX UART1_CTS_B
P146	CAN2_RX_1V8	UART3_TXD	1.8V	UART3_TX UART1_RTS_B
P43	ECSPI1_SS0_1V8	ECSPI1_SS0	1.8V	UART3_RTS_B
P45	ECSPI1_MISO_1V8	ECSPI1_MISO	1.8V	UART3_CTS_B
P56	ECSPI2_SCLK_1V8	ECSPI2_SCLK	1.8V	UART4_RX
P58	ECSPI2_MOSI_1V8	ECSPI2_MOSI	1.8V	UART4_TX
P54	ECSPI2_SS0_1V8	ECSPI2_SS0	1.8V	UART4_RTS_B
P57	ECSPI2_MISO_1V8	ECSPI2_MISO	1.8V	UART4_CTS_B
P140	GPIO9_1V8	UART4_TXD	1.8V	UART4_TX UART2_RTS_B
* For SKUs with an on-board WiFi/BT module, this pin is a NC. This pin is only available for SKUs without an on-board WiFi/BT module.				

Table 4-13: External Signals of UART

5.14 UNIVERSAL SERIAL BUS (USB)

The USB module is a USB 3.0-compliant serial interface engine for implementing a USB interface. This module is connected to an external port. Collectively the module and external port are the USB 3.0 interface. USB 3.0 supports Super-speed (SS), Highspeed (HS), Full-speed (FS), and Low-speed (LS) operations.

- The upper layer is common for USB 2.0 and USB 3.0 operation. This has the bus interface, buffer management block, list processor for scheduling, and control and status register (CSR) functions.
- USB 2.0 PHY and MAC layers
- USB 3.0 PHY, LINK, and MAC layers

The following table describes the external signals of USB:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USB
P62	USB1_OC_1V8	GPIO1_IO13	1.8V	USB1_OC
P63*	USB1_VBUS_3V3	USB1_VBUS	3V3	USB1_VBUS
P64	USB1_ID_1V8	GPIO1_IO10	1.8V	USB1_ID
P61	USB1_D_N	USB1_D_N		USB1_D_N
P60	USB1_D_P	USB1_D_P		USB1_D_P
P48*	USB1_TX_N	USB1_TX_N		USB1_TX_N
P49*	USB1_TX_P	USB1_TX_P		USB1_TX_P
P51*	USB1_RX_N	USB1_RX_N		USB1_RX_N
P52*	USB1_RX_P	USB1_RX_P		USB1_RX_P
* These pins by default are NC but can optionally be connected.				

Table 4-14: External Signals of USB

5.15 ULTRA SECURED DIGITAL HOST CONTROLLER (USDHC)

The Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and the SD/SDIO/MMC cards. The module acts as a bridge, passing host bus transactions to the SD/SDIO/MMC cards by sending commands and performing data accesses to/from the cards. It handles the SD/SDIO/MMC protocols at the transmission level.

The following table describes the external signals of uSDHC:

Pin No.	VEST i.MX 8M Plus SMARC SOM Pin Name	iMX8M Plus Pad Name	Voltage Level	USDHC
P36	SD2_CLK	SD2_CLK	1.8V	USDHC2_CLK
P34*	SD2_CMD	SD2_CMD	1.8V	USDHC2_CMD
P39	SD2_DATA0	SD2_DATA0	1.8V	USDHC2_DATA0
P40	SD2_DATA1	SD2_DATA1	1.8V	USDHC2_DATA1
P41	SD2_DATA2	SD2_DATA2	1.8V	USDHC2_DATA2
P42	SD2_DATA3	SD2_DATA3	1.8V	USDHC2_DATA3
P33	SD2_WP	SD2_WP	1.8V	USDHC2_WP
P35	SD2_nCD	SD2_CD_B	1.8V	USDHC2_CD_B
P37	SD2_RESET_B	SD2_RESET_B	1.8V	USDHC2_RESET_B

Table 4-15: External Signals of uSDHC

5 ELECTRICAL SPECIFICATION

6.1 ABSOLUTE MAXIMUM CHARACTERISTICS

Power Supply Input	Minimum	Maximum
Main Power Supply, DC-IN	-0.3	5.5V

Table 5-1: Absolute Maximum Characteristics

6.2 RECOMMENDED POWER SUPPLY CHARACTERISTICS

Power Supply Input	Minimum	Typical	Maximum	Unit
Voltage of Input Power	4.5	5.0	5.5	V
Current of Input Power		TBD		A

Table 5-2: Recommended Power Supply Characteristics

6.3 POWER CONSUMPTION

The VEST i.MX 8M Plus SOM power consumption is measured in VEST i.MX 8M Plus Carrier Board while running different power scripts under Linux, Yocto.

No.	Power Script	Power Script Operation	I _{max} (A) @ 5.0V Input
1	Power Script 1	LVDS – Play video (H.264) Audio – Headphone in USB – Keyboard and Mouse	TBD
2	Power Script 2	LVDS – Play video (H.264) (foreground) Audio – Headphone in Ethernet – Ping test CPU – Run Stability TEST Utility (background) USB – Keyboard and Mouse	TBD
3	Standby	OS is in idle mode	TBD

Table 5-3: VEST i.MX 8M Plus SOM power consumption

Note:

Power consumption is measured with a standard configuration. For customers that require a custom configuration, overall system design and cooling mechanism need to be addressed by the customer.

Layout Recommendations

This chapter provides recommendations to assist design engineers with the correct layout of their VEST i.MX 8M Plus SOM based systems.

7.1 VEST i.MX 8M PLUS SOM BOARD TRACE LENGTH

Length matching needs to be implemented for each group of high-speed signals. The trace lengths of each SOM board signals are listed below. The designer of the carrier board needs to take note of the trace length on the SOM when performing system signals length matching.

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Trace Length
P1	SMB_ALERT#	SMB_ALERT#_1V8	I	1V8	
P2	GND	GND	Ground	Ground	
P3	CSI1_CK+	CSI1_CK_P	I	Differential	
P4	CSI1_CK-	CSI1_CK_N	I	Differential	
P5	GBE1_SDP	ENET1_CLKI25_3V3	O	3V3	
P6	GBE0_SDP	ENET0_CLKI25_3V3	O	3V3	
P7	CSI1_RX0+	CSI1_D0_P	I	Differential	
P8	CSI1_RX0-	CSI1_D0_N	I	Differential	
P9	GND	GND	Ground	Ground	
P10	CSI1_RX1+	CSI1_D1_P	I	Differential	
P11	CSI1_RX1-	CSI1_D1_N	I	Differential	
P12	GND	GND	Ground	Ground	
P13	CSI1_RX2+	CSI1_D2_P	I	Differential	
P14	CSI1_RX2-	CSI1_D2_N	I	Differential	
P15	GND	GND	Ground	Ground	
P16	CSI1_RX3+	CSI1_D3_P	I	Differential	
P17	CSI1_RX3-	CSI1_D3_N	I	Differential	
P18	GND	GND	Ground	Ground	
P19	GBE0_MDI3-	ETH0_TRX3_N	I/O	Differential	
P20	GBE0_MDI3+	ETH0_TRX3_P	I/O	Differential	
P21	GBE0_LINK100#	ETH0_LED_10_100_3V3_OD	O OD	3V3	
P22	GBE0_LINK1000#	ETH0_LED_1000_3V3_OD	O OD	3V3	
P23	GBE0_MDI2-	ETH0_TRX2_N	I/O	Differential	
P24	GBE0_MDI2+	ETH0_TRX2_P	I/O	Differential	
P25	GBE0_LINK_ACT#	ETH0_LED_ACT_3V3_OD	O OD	3V3	
P26	GBE0_MDI1-	ETH0_TRX1_N	I/O	Differential	
P27	GBE0_MDI1+	ETH0_TRX1_P	I/O	Differential	
P28	GBE0_CTREF	NC	-		
P29	GBE0_MDI0-	ETH0_TRX0_N	I/O	Differential	
P30	GBE0_MDI0+	ETH0_TRX0_P	I/O	Differential	
P31	SPI0_CS1#	NC	-		
P32	GND	GND	Ground	Ground	
P33	SDIO_WP	SD2_WP	I	1V8/3V3	
P34	SDIO_CMD	SD2_CMD	I/O	1V8/3V3	
P35	SDIO_CD#	SD2_nCD	I	1V8/3V3	
P36	SDIO_CK	SD2_CLK	O	1V8/3V3	
P37	SDIO_PWR_EN	SD2_RESET_B	O	1V8/3V3	
P38	GND	GND	Ground	Ground	
P39	SDIO_D0	SD2_DATA0	I/O	1V8/3V3	
P40	SDIO_D1	SD2_DATA1	I/O	1V8/3V3	
P41	SDIO_D2	SD2_DATA2	I/O	1V8/3V3	
P42	SDIO_D3	SD2_DATA3	I/O	1V8/3V3	
P43	SPI0_CS0#	ECSPI1_SS0_1V8	O	1V8	
P44	SPI0_CK	ECSPI1_SCLK_1V8	O	1V8	
P45	SPI0_DIN	ECSPI1_MISO_1V8	I	1V8	
P46	SPI0_DO	ECSPI1_MOSI_1V8	O	1V8	
P47	GND	GND	Ground	Ground	
P48	SATA_TX+	USB1_TX_P*	O	Differential	
P49	SATA_TX-	USB1_TX_N*	O	Differential	
P50	GND	GND	Ground	Ground	
P51	SATA_RX+	USB1_RX_P*	I	Differential	
P52	SATA_RX-	USB1_RX_N*	I	Differential	
P53	GND	GND	Ground	Ground	
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	ECSPI2_SS0_1V8	O	1V8	
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	NC	-		
P56	ESPI_CK / SPI1_CK / QSPI_CK	ECSPI2_SCLK_1V8	O	1V8	
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	ECSPI2_MISO_1V8	I/O	1V8	
P58	ESPI_IO_0 / SPI1_DO / QSPI_IO_0	ECSPI2_MOSI_1V8	I/O	1V8	
P59	GND	GND	Ground	Ground	
P60	USB0+	USB1_D_P	I/O	Differential	
P61	USB0-	USB1_D_N	I/O	Differential	
P62	USB0_EN_OC#	USB1_EN_OC#_3V3	I/O	3V3	
P63	USB0_VBUS_DET	USB1_VBUS_5V0	I	5V0	

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Trace Length
P64	USB0_OTG_ID	USB1_ID_1V8	I	1V8	
P65	USB1+	USB_DN1_D_P	I/O	Differential	
P66	USB1-	USB_DN1_D_N	I/O	Differential	
P67	USB1_EN_OC#	USB_DN1_OC#_3V3	I/O	3V3	
P68	GND	GND	Ground	Ground	
P69	USB2+	USB_DN2_D_P	I/O	Differential	
P70	USB2-	USB_DN2_D_N	I/O	Differential	
P71	USB2_EN_OC#	USB_DN2_EN_OC#_3V3	I/O	3V3	
P72	RSVD	NC	-		
P73	RSVD	NC	-		
P74	USB3_EN_OC#	USB_DN3_EN_OC#_3V3	I/O	3V3	
Key					
P75	PCIE_A_RST#	PCIE_RST#_3V3	O	3V3	
P76	USB4_EN_OC#	USB_DN4_EN_OC#_3V3	I/O	3V3	
P77	PCIE_B_CKREQ#	NC	-		
P78	PCIE_A_CKREQ#	PCI_CLKREQ_B_3V3_OD	I/O OD	3V3	
P79	GND	GND	Ground	Ground	
P80	PCIE_C_REFCK+	NC	-		
P81	PCIE_C_REFCK-	NC	-		
P82	GND	GND	Ground	Ground	
P83	PCIE_A_REFCK+	PCIE_CLK_P	I/O	Differential	
P84	PCIE_A_REFCK-	PCIE_CLK_N	I/O	Differential	
P85	GND	GND	Ground	Ground	
P86	PCIE_A_RX+	PCIE_RX_P	I	Differential	
P87	PCIE_A_RX-	PCIE_RX_N	I	Differential	
P88	GND	GND	Ground	Ground	
P89	PCIE_A_TX+	PCIE_TX_P	O	Differential	
P90	PCIE_A_TX-	PCIE_TX_N	O	Differential	
P91	GND	GND	Ground	Ground	
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P	O	Differential	
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX2_N	O	Differential	
P94	GND	GND	Ground	Ground	
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P	O	Differential	
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX1_N	O	Differential	
P97	GND	GND	Ground	Ground	
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P	O	Differential	
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX0_N	O	Differential	
P100	GND	GND	Ground	Ground	
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TXC_P	O	Differential	
P102	HDMI_CK- / DP1_LANE3-	HDMI_TXC_N	O	Differential	
P103	GND	GND	Ground	Ground	
P104	HDMI_HPD / DP1_HPD	HDMI_HPD_1V8	I	1V8	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL_1V8	I/O OD	1V8	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA_1V8	I/O OD	1V8	
P107	DP1_AUX_SEL	NC	-		
P108	GPIO0 / CAM0_PWR#	CAM0_PWR#_1V8	O	1V8	
P109	GPIO1 / CAM1_PWR#	CAM1_PWR#_1V8	O	1V8	
P110	GPIO2 / CAM0_RST#	CAM0_RST#_1V8	O	1V8	
P111	GPIO3 / CAM1_RST#	CAM1_RST#_1V8	O	1V8	
P112	GPIO4 / HDA_RST#	SDIO_WAKE#_1V8	I	1V8	
P113	GPIO5 / PWM_OUT	PWM_1_1V8	O	1V8	
P114	GPIO6 / TACHIN	TOUCH_INT_1V8	I	1V8	
P115	GPIO7	TOUCH_RST_1V8	I/O	1V8	
P116	GPIO8	CAM0_SYNC_1V8	I/O	1V8	
P117	GPIO9	CAM1_SYNC_1V8	I/O	1V8	
P118	GPIO10	BT_WAKE_1V8	I/O	1V8	
P119	GPIO11	WL_WAKE_1V8	I/O	1V8	
P120	GND	GND	Ground	Ground	
P121	I2C_PM_CK	I2C1_SCL_1V8	I/O I/O	1V8	
P122	I2C_PM_DAT	I2C1_SDA_1V8	I/O I/O	1V8	
P123	BOOT_SELO#	BOOT_MODE0_1V8	I	1V8	
P124	BOOT_SEL1#	BOOT_MODE1_1V8	I	1V8	
P125	BOOT_SEL2#	BOOT_MODE2_1V8	I	1V8	
P126	RESET_OUT#	RESET_OUT#_1V8	O	1V8	
P127	RESET_IN#	RESET_IN_1V8	I OD	1V8	
P128	POWER_BTN#	POWER_BTN	I OD	1V8	
P129	SER0_TX	UART4_TXD_1V8	O	1V8	
P130	SER0_RX	UART4_RXD_1V8	I	1V8	

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Trace Length
P131	SER0_RTS#	UART4_CTS_1V8	O	1V8	
P132	SER0_CTS#	UART4_RTS_1V8	I	1V8	
P133	GND	GND	Ground	Ground	
P134	SER1_TX	UART1_TXD_1V8	O	1V8	
P135	SER1_RX	UART1_RXD_1V8	I	1V8	
P136	SER2_TX	UART2_TXD_1V8*	O	1V8	
P137	SER2_RX	UART2_RXD_1V8*	I	1V8	
P138	SER2_RTS#	UART2_CTS_1V8*	O	1V8	
P139	SER2_CTS#	UART2_RTS_1V8*	I	1V8	
P140	SER3_TX	UART3_TXD_1V8	O	1V8	
P141	SER3_RX	UART3_RXD_1V8	I	1V8	
P142	GND	GND	Ground	Ground	
P143	CAN0_TX	CAN1_TX_1V8	O	1V8	
P144	CAN0_RX	CAN1_RX_1V8	I	1V8	
P145	CAN1_TX	CAN2_TX_1V8	O	1V8	
P146	CAN1_RX	CAN2_RX_1V8	I	1V8	
P147	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P148	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P149	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P150	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P151	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P152	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P153	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P154	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P155	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
P156	VDD_IN	VSYS_5V0	VDD 5V0	5V0	
S1	CSI1_TX+ / I2C_CAM1_CK	I2C2_SCL_1V8	I/O OD	1V8	
S2	CSI1_TX- / I2C_CAM1_DAT	I2C2_SDA_1V8	I/O OD	1V8	
S3	GND	GND	Ground	Ground	
S4	RSVD	NC	-		
S5	CSI0_TX+ / I2C_CAM0_CK	I2C5_SCL_1V8	I/O OD	1V8	
S6	CAM_MCK	CSI_MCLK_1V8	O	1V8	
S7	CSI0_TX- / I2C_CAM0_DAT	I2C5_SDA_1V8	I/O OD	1V8	
S8	CSI0_CK+	CSI2_CK_P	I	Differential	
S9	CSI0_CK-	CSI2_CK_N	I	Differential	
S10	GND	GND	Ground	Ground	
S11	CSI0_RX0+	CSI2_D0_P	I	Differential	
S12	CSI0_RX0-	CSI2_D0_N	I	Differential	
S13	GND	GND	Ground	Ground	
S14	CSI0_RX1+	CSI2_D1_P	I	Differential	
S15	CSI0_RX1-	CSI2_D1_N	I	Differential	
S16	GND	GND	Ground	Ground	
S17	GBE1_MDIO+	ETH1_TRX0_P	I/O	Differential	
S18	GBE1_MDIO-	ETH1_TRX0_N	I/O	Differential	
S19	GBE1_LINK100#	ETH1_LED_10_100_3V3_OD	O OD	3V3	
S20	GBE1_MDI1+	ETH1_TRX1_P	I/O	Differential	
S21	GBE1_MDI1-	ETH1_TRX1_N	I/O	Differential	
S22	GBE1_LINK1000#	ETH1_LED_1000_3V3_OD	O OD	3V3	
S23	GBE1_MDI2+	ETH1_TRX2_P	I/O	Differential	
S24	GBE1_MDI2-	ETH1_TRX2_N	I/O	Differential	
S25	GND	GND	Ground	Ground	
S26	GBE1_MDI3+	ETH1_TRX3_P	I/O	Differential	
S27	GBE1_MDI3-	ETH1_TRX3_N	I/O	Differential	
S28	GBE1_CTREF	NC	-		
S29	PCIE_D_TX+ / SERDES_0_TX+	CSI2_D2_P*	O	Differential	
S30	PCIE_D_TX- / SERDES_0_TX-	CSI2_D2_N*	O	Differential	
S31	GBE1_LINK_ACT#	ETH1_LED_ACT*_3V3_OD	O	3V3	
S32	PCIE_D_RX+ / SERDES_0_RX+	CSI2_D3_P*	I	Differential	
S33	PCIE_D_RX- / SERDES_0_RX-	CSI2_D3_N*	I	Differential	
S34	GND	GND	Ground	Ground	
S35	USB4+	USB4_DN4_D_P	I/O	Differential	
S36	USB4-	USB4_DN4_D_N	I/O	Differential	
S37	USB3_VBUS_DET	NC	-		
S38	AUDIO_MCK	SAI2_MCLK_1V8	O	1V8	
S39	I2S0_LRCK	SAI2_TXFS_1V8	I/O	1V8	
S40	I2S0_SDOUT	SAI2_TXD_1V8	O	1V8	
S41	I2S0_SDIN	SAI2_RXD_1V8	I	1V8	
S42	I2S0_CK	SAI2_TXC_1V8	I/O	1V8	
S43	ESPI_ALERT0#	NC	-		
S44	ESPI_ALERT1#	NC	-		

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Trace Length
S45	MDIO_CLK	NC	-		
S46	MDIO_DAT	NC	-		
S47	GND	GND	Ground	Ground	
S48	I2C_GP_CK	I2C4_SCL_1V8	I/O	1V8	
S49	I2C_GP_DAT	I2C4_SDA_1V8	I/O	1V8	
S50	HDA_SYNC / I2S2_LRCK	SAI3_TXFS_1V8	I/O	1V8	
S51	HDA_SDO / I2S2_SDOUT	SAI3_TXD_1V8	O	1V8	
S52	HDA_SDI / I2S2_SDIN	SAI3_RXD_1V8	I/O	1V8	
S53	HDA_CK / I2S2_CK	SAI3_TXC_1V8	O	1V8	
S54	SATA_ACT#	NC	-		
S55	USB5_EN_OC#	NC	-		
S56	ESPI_IO_2 / QSPI_IO_2	NC	-		
S57	ESPI_IO_3 / QSPI_IO_3	NC	-		
S58	ESPI_RESET#	NC	-		
S59	USB5+	NC	-		
S60	USB5-	NC	-		
S61	GND	GND	Ground	Ground	
S62	USB3_SSTX+	USB_DN3_SSTX_P	O	Differential	
S63	USB3_SSTX-	USB_DN3_SSTX_N	O	Differential	
S64	GND	GND	Ground	Ground	
S65	USB3_SSRX+	USB_DN3_SSRX_P	I	Differential	
S66	USB3_SSRX-	USB_DN3_SSRX_N	I	Differential	
S67	GND	GND	Ground	Ground	
S68	USB3+	USB_DN3_D_P	I/O	Differential	
S69	USB3-	USB_DN3_D_N	I/O	Differential	
S70	GND	GND	Ground	Ground	
S71	USB2_SSTX+	USB_DN2_SSTX_P	O	Differential	
S72	USB2_SSTX-	USB_DN2_SSTX_N	O	Differential	
S73	GND	GND	Ground	Ground	
S74	USB2_SSRX+	USB_DN2_SSRX_P	I	Differential	
S75	USB2_SSRX-	USB_DN2_SSRX_N	I	Differential	
S76	PCIE_B_RST#	NC	-		
Key					
S77	PCIE_C_RST#	NC	-		
S78	PCIE_C_RX+ / SERDES_1_RX+	EARC_N_HPDP	I/O	1V8	
S79	PCIE_C_RX- / SERDES_1_RX-	EARC_P_UTIL	I/O	1V8	
S80	GND	GND	Ground	Ground	
S81	PCIE_C_TX+ / SERDES_1_TX+	EARC_AUX	I/O	1V8	
S82	PCIE_C_TX- / SERDES_1_TX-	EHDMA_CEC	I/O	1V8	
S83	GND	GND	Ground	Ground	
S84	PCIE_B_REFCK+	NC	-		
S85	PCIE_B_REFCK-	NC	-		
S86	GND	GND	Ground	Ground	
S87	PCIE_B_RX+	NC	-		
S88	PCIE_B_RX-	NC	-		
S89	GND	GND	Ground	Ground	
S90	PCIE_B_TX+	NC	-		
S91	PCIE_B_TX-	NC	-		
S92	GND	GND	Ground	Ground	
S93	DPO_LANE0+	NC	-		
S94	DPO_LANE0-	NC	-		
S95	DPO_AUX_SEL	NC	-		
S96	DPO_LANE1+	NC	-		
S97	DPO_LANE1-	NC	-		
S98	DPO_HPDP	NC	-		
S99	DPO_LANE2+	NC	-		
S100	DPO_LANE2-	NC	-		
S101	GND	GND	Ground	Ground	
S102	DPO_LANE3+	NC	-		
S103	DPO_LANE3-	NC	-		
S104	USB3_OTG_ID	NC	-		
S105	DPO_AUX+	NC	-		
S106	DPO_AUX-	NC	-		
S107	LCD1_BKLT_EN	LVDS1_BKLT_EN_1V8	O	1V8	
S108	LVDS1_CLK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	I/O	Differential	
S109	LVDS1_CLK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	I/O	Differential	
S110	GND	GND	Ground	Ground	
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_TX0_P	O	Differential	

Pin No.	SMARC Pin Name	Signal name	Signal Type	Voltage Level	Trace Length
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_TX0_N	O	Differential	
S113	eDP1_HPD / DSI1_TE	NC	-		
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_TX1_P	O	Differential	
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_TX1_N	O	Differential	
S116	LCD1_VDD_EN	LVDS1_VDD_EN_1V8	O	1V8	
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_TX2_P	O	Differential	
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_TX2_N	O	Differential	
S119	GND	GND	Ground	Ground	
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_TX3_P	O	Differential	
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_TX3_N	O	Differential	
S122	LCD1_BKLT_PWM	PWM_3_1V8	O	1V8	
S123	GPIO13	HP_DETECT_1V8	I/O	1V8	
S124	GND	GND	Ground	Ground	
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_DSI0_TX0_P	O	Differential	
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_DSI0_TX0_N	O	Differential	
S127	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_BKLT_EN_1V8	O	1V8	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_DSI0_TX1_P	O	Differential	
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_DSI0_TX1_N	O	Differential	
S130	GND	GND	Ground	Ground	
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_TX2_P	O	Differential	
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_TX2_N	O	Differential	
S133	LCD0_VDD_EN	LVDS0_VDD_EN_1V8	O	1V8	
S134	LVDS0_CLK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_DSI0_CLK_P	O	Differential	
S135	LVDS0_CLK- / eDP0_AUX- / DSI0_CLK-	LVDS0_DSI0_CLK_N	O	Differential	
S136	GND	GND	Ground	Ground	
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_SDI0_TX3_P	O	Differential	
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_SDI0_TX3_N	O	Differential	
S139	I2C_LCD_CLK	I2C3_SCL_1V8	I/O	1V8	
S140	I2C_LCD_DAT	I2C3_SDA_1V8	I/O	1V8	
S141	LCD0_BKLT_PWM	LCD0_PWM2_1V8	O	1V8	
S142	GPIO12	RTC_INT_1V8	I/O	1V8	
S143	GND	GND	Ground	Ground	
S144	eDP0_HPD / DSI0_TE	NC	-		
S145	WDT_TIME_OUT#	WDOG_B_1V8	O	1V8	
S146	PCIE_WAKE#	PCIE_WAKE#_3V3	I	3V3	
S147	VDD_RTC	NC	-		
S148	LID#	LID#_1V8	I	1V8	
S149	SLEEP#	SLEEP#_1V8	I	1V8	
S150	VIN_PWR_BAD#	VIN_PWR_BAD#_1V8	I	1V8	
S151	CHARGING#	CHARGING#_1V8	I	1V8	
S152	CHARGER_PRSENT#	CHARGER_PRSENT#_1V8	I	1V8	
S153	CARRIER_STBY#	CARRIER_STBY#_1V8	O	1V8	
S154	CARRIER_PWR_ON	CARRIER_PWR_ON_1V8	O	1V8	
S155	FORCE_RECOV#	FORCE_RECOV#_1V8	I	1V8	
S156	BATLOW#	BATLOW#_1V8	I	1V8	
S157	TEST#	NC	-	-	
S158	GND	GND	GROUND	GROUND	

Table 5-4: Trace Length of SO-DIMM Signals

7.2 PCI EXPRESS INTERFACE RECOMMENDATIONS

Use the following recommendations for PCI Express interface:

- PCIe differential pairs should have a differential impedance of $85\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.
- Match the signals with respect to PCIE_CLK (clock signal) ± 50 mils.

7.3 LVDS RECOMMENDATIONS

Use the following recommendations for the LVDS:

- LVDS differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.

- Match the signals with respect to LVDS_CLK (clock signal) ± 50 mils.

7.4 USB RECOMMENDATIONS

Use the following recommendations for the USB:

- The differential pairs should have a differential impedance of $90\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.

7.5 MIPI CSI RECOMMENDATIONS

Use the following recommendations for the MIPI CSI:

- The differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.
- Match the signals with respect to CSI_CLK (clock signal) ± 25 mils.

7.6 MIPI DSI RECOMMENDATIONS

Use the following recommendations for the MIPI DSI:

- The differential pairs should have a differential impedance of $100\Omega \pm 10\%$.
- Each differential pair should be length matched to ± 5 mils.
- Match the signals with respect to CSI_CLK (clock signal) ± 25 mils.

7.7 SD INTERFACE RECOMMENDATIONS

Use the following recommendations for the SD interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$.
- Match the signals with respect to SDx_CLK (clock signal) ± 50 mils.

7.8 SAI RECOMMENDATIONS

Use the following recommendations for the I2S interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$.
- Match the signals with respect to clock signal ± 100 mils.

7.9 SPI INTERFACE RECOMMENDATIONS

Use the following recommendations for the SPI interface:

- Trace impedance for all signals is $50\Omega \pm 10\%$.
- Match the signals with respect to SPI_CLK (clock signal) ± 50 mils.

7.10 ENET INTERFACE RECOMMENDATIONS

Use the following recommendations for the ENET interface:

- Trace impedance for each differential pair is $100\Omega \pm 10\%$.
- Within the differential signals, match the signals ± 5 mils.
- Same pair P/N skew should be less than 20 mils.

- *Match the signals with respect to ENET_REF_CLK_50M (clock signal) ± 100 mils.*
- *The length for each differential pair should be a maximum of 4 inches.*

7.11 HDMI RECOMMENDATIONS

Use the following recommendations for the HDMI interface:

- *Trace impedance for each differential pair is $100\ \Omega \pm 10\%$.*
- *Within the differential signals, match the signals ± 5 mils.*

Match the signals with respect to HDMI_CLK (clock signal) ± 50 mils.

6 ENVIRONMENTAL SPECIFICATION

6.1 TEMPERATURE SPECIFICATION

The VEST SMARC i.MX 8M Plus SOM has multiple SKUs with some configurations available with different operating temperatures.

Note: The VEST i.MX 8M Plus SMARCSOM comes in different operating temperature grade of the SOM components. Nevertheless, customers should consider specific thermal design for the final product and the specific operating environment and operational conditions. Increased temperatures affect the longevity of the parts.

6.2 HUMIDITY

- *Operating: 10% to 90% (Non-condensing)*
- *Non-operating: 5% to 95% (Non-condensing)*

7 MECHANICAL SPECIFICATION

7.1 MECHANICAL DIMENSION

- 82 mm x 50 mm

7.2 MECHANICAL DRAWING

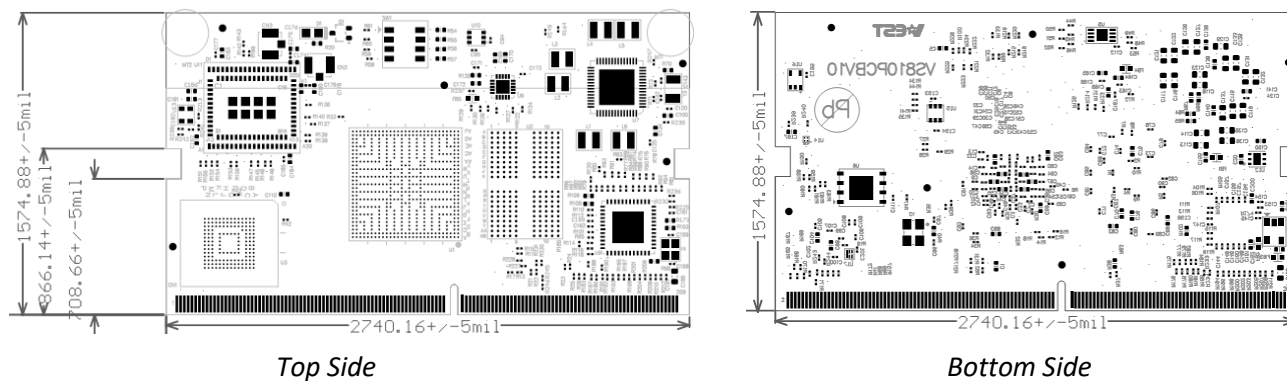


Figure 7-1: Mechanical Drawing

8 REVISION HISTORY

Version	Date Released	Changes
<i>A</i>	<i>04/04/24</i>	<i>Initial Release</i>
<i>B</i>	<i>06/05/24</i>	<i>Updated Photos and minor corrections</i>
<i>C</i>	<i>07/24/24</i>	<i>Minor Corrections and Updates</i>

9 LEGAL NOTICES

The signed agreement between Purchaser and APC will govern the sale and purchase of APC's Venture Embedded Solutions Technology ("VEST") products ("Products"). In the event that no agreement has been concluded, APC's terms and conditions of supply will apply.

Testing and other quality control techniques are used to the extent that APC deems necessary to support its warranty.

Except where required by law, specific testing of all parameters of each Product is not necessarily performed.

Purchaser must provide adequate design and operating safeguards to minimize inherent or procedural and technical risks associated with Purchaser products and applications. Purchaser is solely responsible for its selection and use of APC Products. APC assumes no liability for applications assistance, Purchaser product design or any incompatibility of the Product with Purchaser product.

Products supplied by APC are not designed, intended or authorized for use in life support, life sustaining, medical systems or devices, aircraft navigation, nuclear, or other applications, including, but not limited to, public transportation operating systems, in which the failure of such Products could reasonably be expected to result in personal injury, loss of life or severe property or environmental damage. Purchaser acknowledges that use of APC's Products in such product applications is understood to be fully at the risk of Purchaser and that Purchaser is responsible for verification and validation of the suitability of APC's Products in such applications. Purchaser agrees that APC is not and shall not be liable, in whole or in part, for any claim or damage arising from use in such applications. Purchaser agrees to indemnify, defend and hold APC harmless from and against any and all claims, damages, losses, costs, expenses and liabilities arising out of or in connection with any such use or application.

APC retains all rights to all proprietary intellectual property in the Products and associated manufacturing processes and has the right to file for and obtain intellectual property protection for same.